International Journal of Robotics and Control Systems
Vol. 5, No. 6, 2025, pp. 3395-3412
ISSN 2775-2658
http://pubs2.ascee.org/index.php/ijrcs

Modified Doherty Power Amplifier with Hybrid Current-Voltage Amplification for High-Efficiency Broadband Applications

Ahmad A. Ismael [a,1], Mohammad Tariq Yaseen [a,b,2,*]

[a] Department of Electrical Engineering Collage of Engineering, University of Mosul, Mosul, 00964, Iraq
[b] Department of Communications and Intelligent Digital Systems Engineering, Collage of Engineering, University of Mosul, Mosul, 00964, Iraq
[1] a.a.ismail@uomosul.edu.iq; [2] mtyaseen@uomosul.edu.iq
* Corresponding Author

ARTICLE INFO

Article history
Received August 26, 2025
Revised October 25, 2025
Accepted December 31, 2025

Keywords
Class-E-Switching;
Load Modulation;
Linearity;
IMD;
5G Application

ABSTRACT

There is an urgent need to improve the performance of power amplifiers in modern communication system applications in terms of linearity, efficiency, and output power to ensure performance that meets the requirements of these applications. This research contributed to developing a switched-mode hybrid amplifier that simultaneously combines current and voltage amplification by modifying both the main and auxiliary amplifiers in the Doherty power amplifier, merging their output power through a load modulation network, and applying this combined power to the load. The characteristics of the hybrid amplifier enable an increase in efficiency and gain and an enhancement in output power, while the load modulation network achieves an ideal matching that contributes to improving the linearity of the amplifier. The suggested amplifier was modeled with the ADS simulation program. The simulation results at a frequency of 850 MHz were an output power of 38 dBm, a power-added efficiency of 71.3%, a dynamic range of 12 dB, and a power gain of 23 dB in the single-tone test. As for the results of the amplifier test for a two-tone signal with a bandwidth of 100 MHz, the output power was 29.5 dBm, the additional power efficiency was 30%, and the power gain was 17 dB. The results indicate that the suggested power amplifier is appropriate for implementation in fifth-generation communication system transmitters.

1. Introduction

Power combining is a technique used in various fields of electronics and communications to increase the total output power by combining power from multiple sources. This technology is particularly important in applications such as radar systems, satellite communications, and wireless transmission, where high power is required to efficiently transmit signals over long distances. In advanced generation communication systems, power combining devices require wide bandwidth and high linearity due to the nature of the signal, which has a wide bandwidth and high Peak-to-Average Power Ratio (PAPR) [1]–[4]. Many researchers have used various techniques to overcome manufacturing challenges such as parasitic components and breakdown voltages, which reduce power

output and limit the amplifier's bandwidth [5]–[8]. Therefore, new technologies have been developed in modern communications systems to overcome this problem, including stacked amplifiers and distributed power amplifiers [9]–[13]. There are other techniques used to avoid the most significant problem facing traditional power combining technology, namely the need to use a large number of transistors connected in parallel. Increasing the number of transistors leads to an increase in the effect of parasitic capacitances, thereby reducing the output impedance, which affects the linearity of the amplifier and decreases the bandwidth [14]. Many studies have addressed the use of various techniques for power amplification with the aim of improving the linearity and bandwidth of the amplifier to suit the applications of digital signal modulation systems for advanced generations of communications. In [15], the authors propose a novel dual-mode power amplifier architecture employing a low-loss parallel power-combining transformer (PCT) that enables efficient load modulation and intrinsic third-order intermodulation (IMD3) cancellation. The dual-mode operation allows dynamic switching between high-power and low-power modes, optimizing current consumption based on output requirements. The implemented design, based on InGaP/GaAs HBT technology and tested at 0.91 GHz, achieved a peak output power of 33.8 dBm with a power-added efficiency of 54.5%, while maintaining excellent linearity. These results show that the suggested PCT-based combining and IMD3 suppression methods work well for high-performing power amplifiers.

Innovative asymmetric Doherty power amplifier (DPA) architecture was used instead of the traditional DPA technique to enhance both efficiency and output power while maintaining linearity and broadband capability [16]. The authors present an innovative asymmetric DPA architecture that employs carrier and peaking amplifiers of different cell sizes and integrates a complex combining load (CCL) network to facilitate efficient load modulation over the combining node. the amplifier achieved a saturated output power of 43.5 dBm at 1.68 GHz. The results confirm that the asymmetric cell sizing combined with a complex load network effectively improves efficiency and linearity across both saturation and back-off operating regimes, making the approach suitable for high-performance wireless applications.

The article [17], tackles the significant issue of attaining wideband functionality, elevated efficiency, and linearity in sub-6 GHz (5G) power amplifiers. The authors propose a continuous mode Doherty design executed in a 250-nm GaN MMIC process to address limited bandwidth. The design uses a simple impedance inverter network made with basic components to maintain the impedance in both back-off and saturation states, allowing wideband Doherty combining.

Previous studies have indicated that researchers have focused on improving power amplifier performance by amplifying voltage, or current, using various amplifier topologies. Although voltage and current amplifiers each have distinct characteristics, combining them in a single amplifier is a challenging option due to the different input and output impedance characteristics of the two amplifiers, which makes it difficult to combine their power into a common load. This research addresses the modification of a Doherty power amplifier using a hybrid amplifier consisting of a main and auxiliary amplifier to simultaneously amplify current and voltage. The Doherty power amplifier and load modulation techniques combine the outputs of both amplifiers to deliver power to the load. This approach achieves high power gain. Thanks to the load modulation circuit, the amplifier's output impedance is close to the load impedance, reducing the impedance matching ratio. This, in turn, reduces the effect of parasitic capacitors and improves the amplifier's linearity and increases its bandwidth. To increase the efficiency of the proposed amplifier, an E-type switching amplifier was used in both the main and auxiliary amplifiers. The researchers constructed and modified the basic Doherty amplifier to produce a modular Doherty power amplifier (MDPA) using advanced simulation software (ADS) to demonstrate the effectiveness of this new technology in achieving high gain and output power through modifications to the amplifier components. The test results for the proposed amplifier compared to the basic amplifier were as follows. The linearity improved by 4 dB as measured by third harmonic distortion (THD), while the gain was 23 dB, an increase of 2 dB. The output power was 38 dB, an increase of 5 dB. The power-added efficiency and dynamic range of the proposed amplifier were 71% and 12 dB, respectively. Through the results that were reached, it became clear that the research objectives were achieved satisfactorily in terms of efficiency, linearity,

gain, and output capacity. The results indicate that the Modified Doherty Power Amplifier (MDPA) represents a potential alternative for building power amplifiers in contemporary 5G communication systems and Internet of Things (IoT) network transmitters. The amplifier's linearity and wide bandwidth also make it suitable for use in remote control devices and machine-to-machine (M2M) communication systems.

2. Theoretical Basics

This research includes a new concept aimed at achieving high power amplification with appropriate linearity and efficiency by combining the power generated by two amplifiers with different input and output impedances and different power amplification values. Combining power from two amplifiers with different characteristics is challenging due to the possibility of mismatch between the amplifiers in the power combination circuit, which may hinder effective power combining. Therefore, the principle of load modulation and the Doherty amplifier were adopted to achieve a power combination for this type of amplifier. The final construction of the proposed amplifier enables a power combination of the two different amplifiers. Therefore, we will discuss the theoretical basis of the concept of load modulation and the Doherty amplifier to gain an understanding of the proposed amplifier's basic operation.

2.1. Impedance Modulation Concepts

The core principle of impedance transformation is that the load impedance of a current source may be modified by introducing a current from a supplementary current source. Analyze the circuit depicted in Fig. 1 [2], [18], [19].

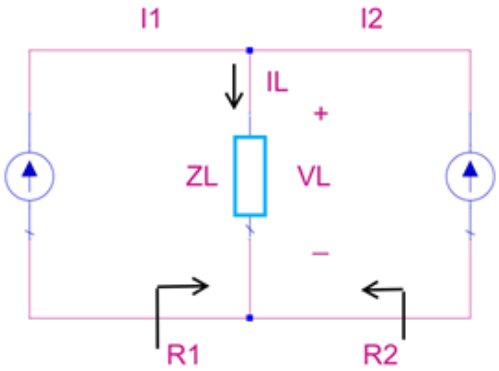


Fig. 1. Circuit diagram represents load impedance modulation

The present source I_1 signifies the transistor of a power amplifier operating as a current source. Similarly, the present source I_2 denotes the transistor of an auxiliary power amplifier operating as a current source. In accordance with Kirchhoff's current law,

$$I_L = I_1 + I_2 \tag{1}$$

According to Ohm's law,

$$R_L = {}^{V}/_{I_L} \tag{2}$$

The load impedance observed by the current sources I_1 is

$$R_1 = \frac{V}{I_1} = \frac{V}{I_L - I_2} = \frac{V}{I_L\left(1 - \frac{I_2}{I_L}\right)} = \frac{V}{I_L\left(1 - \frac{I_2}{I_1 + I_2}\right)} = R_L\left(1 + \frac{I_2}{I_1}\right) \tag{3}$$

As a result, the load resistance that is seen by the current source I_1 is proportional to the current I_2. It is possible for the load voltage V to grow when the currents I_1 and I_2 are in phase with one

another. As a result, the current source I_1 will experience a larger load resistance, For $I_2 = I_1$, $R_1 = 2R_L$. For $I_2 = 0$ the $R_1 = R_L$.

Similarly, the load resistance of the current source I_2 is expressed as

$$R_2 = \frac{V}{I_2} = R_L\left(1 + \frac{I_1}{I_2}\right) \tag{4}$$

From Fig. 1, (3), and (4), it is shown that the impedance transformation or load modulation technique allows the output power from the two sources to be transferred, even if their impedances are different.

2.2. Doherty Power Amplifier Concepts

The concept of the Doherty power amplifier (DPA) is fundamental to implementing the research idea, which includes two main axes: load modulation and power combining. Fig. 2 shows the general schematic and equivalent circuit of the Doherty amplifier [20]. Doherty Amplifier compromises of two amplifiers: the Main (carrier) amplifier and the Auxiliary (peaking) amplifier [21], [22]. In the conventional Doherty Power Amplifier, the Main and Auxiliary amplifiers are inherently biased in Class AB and C modes, respectively. The gate bias voltage of the auxiliary amplifier is chosen to be lower than that of the Main amplifier to active the auxiliary amplifier at back-off power (BOP) [17], [23], [24]. A quarter-wavelength (λ/4) transmission line TL1 or impedance inverter connects the outputs of the main amplifiers to the common load. This network enables load modulation, allowing the main amplifier to see a changing impedance depending on the auxiliary's activity. The transmission line TL2 before the auxiliary amplifier provides phase compensation, aligning its signal with the phase-shifted output of the main amplifier due to the λ/4 line, which is essential for correct in-phase power combining and high efficiency. The third transmission line's (TL3) function is to combine power from the load modulator circuit and send it to the 50-ohm output impedance [25].

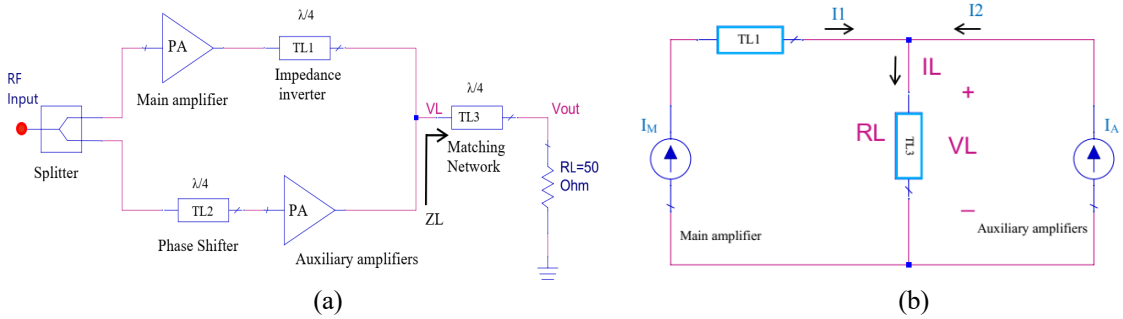


Fig. 2. (a) General schematic of the DPA (b) equivalent circuit of DPA

The output power of the Doherty power amplifier can be obtained from the following equation:

$$P_{out} = (I_M + I_A)^2 . RL \tag{5}$$

The equation in (5) illustrates that increasing the current gain in the main amplifier can obtain a larger output current for the main amplifier, thus doubling the output power in proportion to the square of the current, according to the equation above. This differs from traditional methods of combining power, where the output power is proportional to the number of amplifiers connected in parallel [26]–[28].

3. Realization the Proposed Power Amplifier

This research proposes a new Doherty power amplifier architecture. The goal of this research is to build an amplifier capable of producing high power with linearity and efficiency suitable for use in modern communications systems. Several modifications were made to improve the Doherty power amplifier to suit its intended use.

1. To enhance amplifier efficiency, a switching amplifier was employed in both the main and auxiliary amplifiers, rather than utilizing traditional amplifiers.
2. A high-voltage gain amplifier had been used in the auxiliary amplifier, while a high-current gain amplifier had been used in the main amplifier to increase output power through simultaneous voltage and current.
3. Making both the main and auxiliary amplifiers operate at the same voltage bias ensures continuous operation across all power levels. This improvement enhances the amplifier's linearity by reducing its sensitivity to changes in bias voltage and eliminating the switching glitch [21], [29].
4. To double the current gain of the main amplifier, two amplifiers with the same current gain are connected in parallel. Connecting the amplifiers in parallel allows them to handle a wider current range, which doubles the current gain and boosts the output power based on the combined current gain of the amplifiers. This is because power is proportional to the square of the current.
5. The proposed amplifier depends on optimal power distribution between the main and auxiliary amplifiers to attain ideal performance, specifically in regulating the current ratio, establishing the output impedances, and determining the gain through the characteristic impedance values of the transmission lines depicted in Fig. 2(a) [29].
6. Match the output of both the main and auxiliary amplifiers to the standard 50-ohm impedance before the collector point at the input of the TL3 transmission line to improve the linearity of the amplifier and increase the bandwidth.

This idea can be applied to different types of amplifiers, but our research will focus on the Class E amplifier, which is a basic block in the modified Doherty amplifier. The Class E amplifier is pre-designed, and its performance has been determined through computer simulations of the amplifier [30].

In this paper, a gallium arsenide (GaAs) field-effect transistor (FET) was chosen to build the proposed amplifier. The GaAs power amplifier achieves a balance between efficiency, linearity, and thermal stability. Thanks to its high electron mobility and wide bandgap, GaAs enables high-frequency operation with low noise, superior linearity, high output power, and efficiency, making it ideal for 5G networks at frequencies below 6 GHz and Wi-Fi networks [31]–[33]. The design of the proposed power amplifier, which operates at 850 MHz and uses a GaAs FET model, went through several stages that applied the previously mentioned points to achieve the final amplifier. The first stage was the design of the Doherty power amplifier (PA1) based on E-type power amplifier such that both the main and auxiliary amplifiers were E-type in order to improve the amplifier performance in terms of efficiency. The main amplifier bias was set to -2.4 V (VG) and the auxiliary amplifier bias was set to -3.2 V (VG) after analyzing the current-voltage (I, V) characteristics of the CaAs transistor. The first model was then modified to avoid the switching glitch problem by making the main and auxiliary amplifiers operate at all times. This amplifier was called the symmetrical Doherty amplifier (PA2) with symmetrical bias of both amplifiers at (VG = -2.4 V).

The final step in the final design (PA3) is to connect two amplifiers in parallel to double the current gain and form the main amplifier in the modified DPA. In high-power amplifier design, connecting multiple transistors in parallel is a well-established approach to increase the overall output power without exceeding the safe operating limits of a single device. Instead of using a physically larger transistor, which increases parasitic capacitances, reduces gain, and limits bandwidth, parallel connection allows designers to share current, distribute heat, and maintain better impedance matching at high frequencies [34]–[38]. To reduce the size of the amplifier, the minimum number of amplifiers connected in parallel was used, which is only two amplifiers. The proposed amplifier (PA3) in its final form can be named the Modified Doherty Power Amplifier (MDPA). Fig. 3 shows the final model of the power amplifier (MDPA).

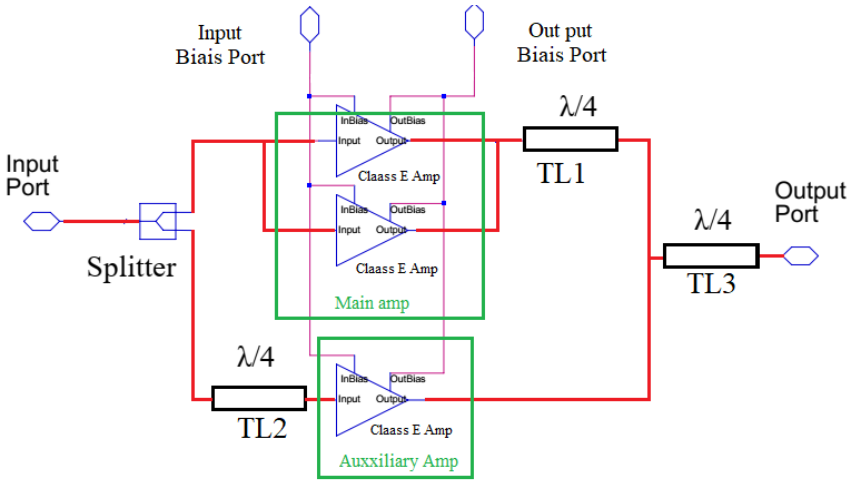


Fig. 3. General schematic of Modified Doherty Power Amplifier (MDPA)

The flowchart shown in Fig. 4 illustrates the stages of building the proposed amplifier and the methodology followed to reach the final assembly (MDPA).

4. The Simulation Results

Preparing the appropriate operating point is one of the important factors in the success of the amplifier function. Since the function of the main or carrier amplifier in the proposed amplifier is current amplification, it was important to choose the bias point so that the current swings over a wide range to achieve high current gain, while the focus in the secondary amplifier is on voltage amplification, resulting in less current swing. Fig. 5 represents the output characteristics of both the main and Auxiliary amplifiers in the proposed amplifier.

Many tests were conducted to evaluate the amplifier's performance under different working conditions and to assess the amplifier's effectiveness based on the amplifier's performance in those tests. The tests were arranged as follows.

4.1. S-Parameters Simulation

S-Parameters simulation test provides a suitable environment for studying the amplifier's characteristics as frequency changes, based on the response of the scattering parameters and reflection coefficients. Based on the values of these variables, the amplifier's stability is checked and the noise factor is calculated under operating conditions. The amplifier is evaluated based on (6) and (7):

$$K = \frac{(1 - |S11|^2 - |S22|^2 + |\Delta|^2)}{(2 * |S12 * S21|)} \tag{6}$$

$$\Delta = S11 * S22 - S12 * S21 \tag{7}$$

In this context, K represents the stability factor, while S11, S22, S21, and S12 are referred to as the scattering parameters. According to the results obtained Fig. 6(a), an amplifier is considered unconditionally stable when K > 1 and Delta = |Δ| < 1 [39], [40]. These criteria ensure stability regardless of the source or load impedances—important for broadband or high-power designs [41]–[43]. Another thing that was obtained by examining the S-parameters is the noise figure, which is considered very suitable for this design because its value in the work area is less than 5 dB [44], [45]. Fig. 6(b) shows the examination results of Noise figure. The responses of forward reflection (S11) and reverse reflection (S22) as a function of frequency on the Smith Chart confirm this behavior across a broad frequency range, spanning from 0.5 GHz to 1 GHz, as both S11 and S22 reside within the confines of the Smith Chart circle, as depicted in Fig. 7.

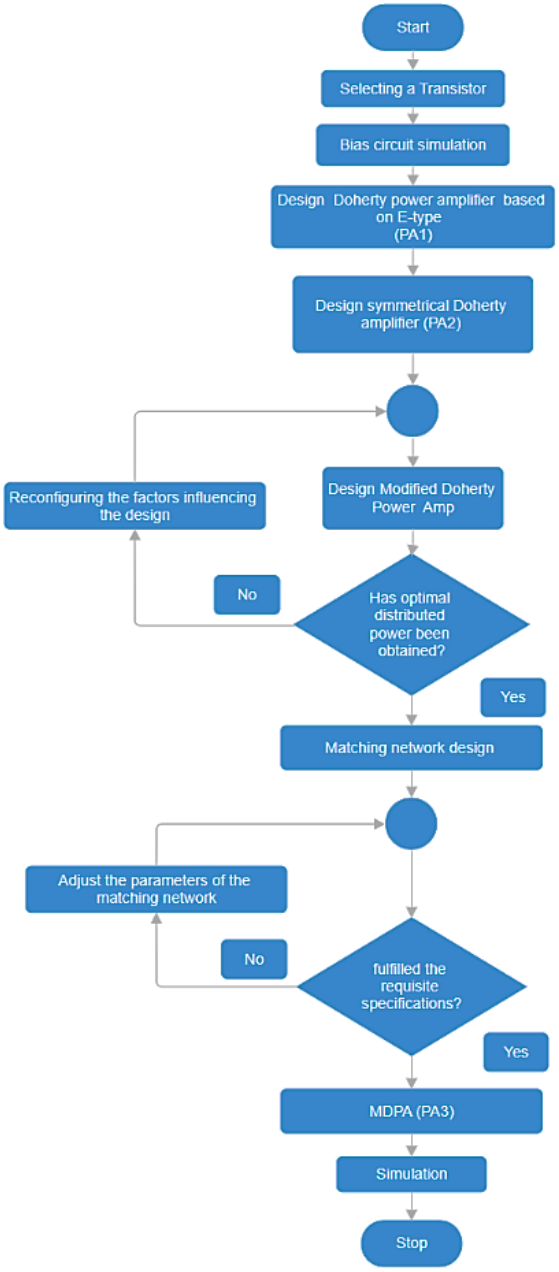
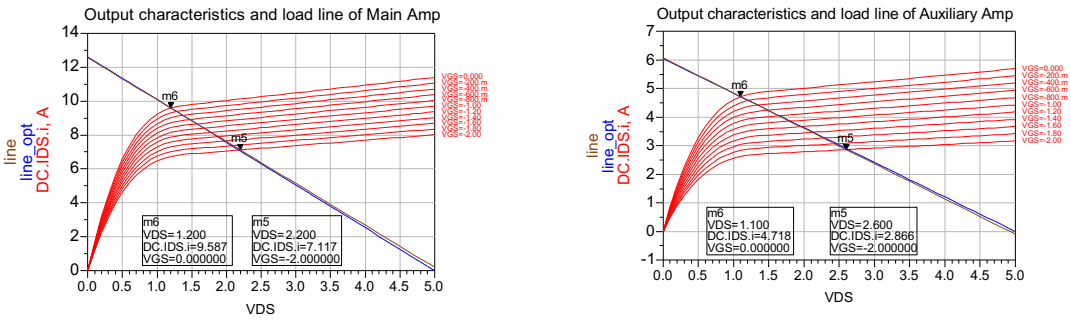


Fig. 4. A general diagram of the methodology used in designing the proposed amplifier



(a) (b)

Fig. 5. Output characteristics and load line: (a) Main Amp; (b) Auxiliary Amp

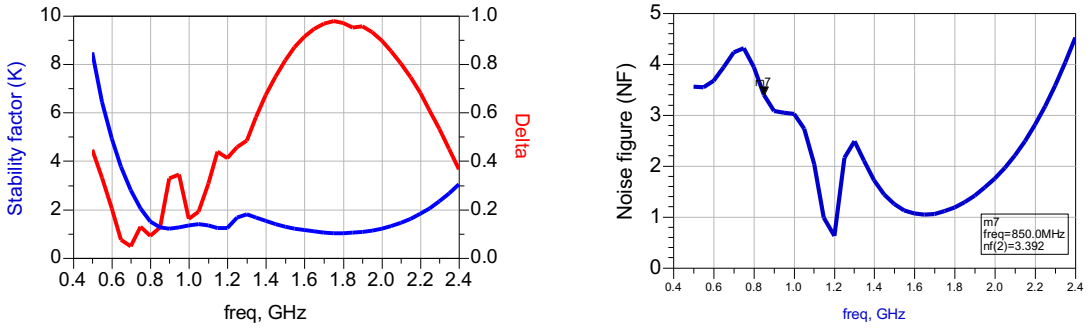


Fig. 6. S-Parameters simulation test results: (a) Stability barometer K, Δ; (b) Noise figure

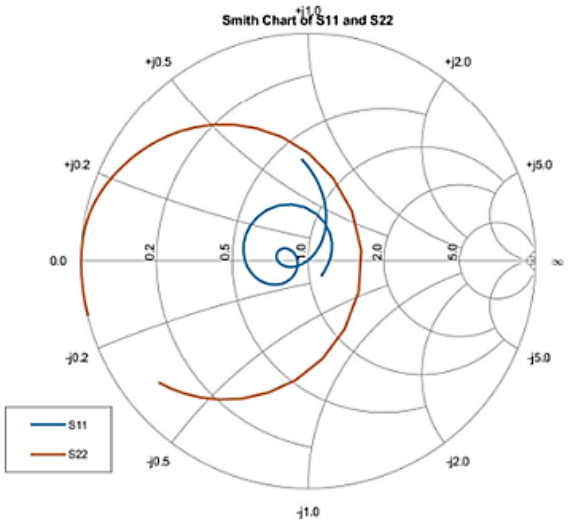


Fig. 7. Response of reflection coefficients S11 and S22 as a function of frequency

4.2. One Tone Harmonic Balance

Single tone analysis involves examining both the time and frequency domains to assess an amplifier's response to a test signal at its operating frequency, thereby providing insights into the amplifier's gain, efficiency, and linearity, this also includes the distribution of the power spectrum at the amplifier's output. The power allocation between the auxiliary and main amplifiers is an important matter in all design stages, starting from the basic design (PA1) and reaching the final amplifier (PA3), because it determines the current of each amplifier, the power gain, and the output impedance. The proposed amplifier was tested through a single-tone test at a frequency of 850 MHz to evaluate the amplifier's performance through the results obtained.

Fig. 8 shows the relation between output power in watts and input RF power in dBm and the contribution of both the carrier (Main) and peaking (Auxiliary) amplifiers in producing power. Fig. 8(a) illustrates the variation in output power and power added efficiency (PAE) as a consequence of input power alterations. We also can see from the Fig. 8(a) that the amplifier has a constant gain over a wide range of input power changes, indicating the amplifier has high linearity to the signal, which has wide amplitude variation. Through the compression point indicated by the line marker, it was found that the highest output power equals 38 dBm and the power added efficiency equals 71.3%. Fig. 8(b) represents the output power on the Y axis and the output power on the Right Y axis and shows the continuity of power production for both the main and auxiliary amplifiers over the entire range of input power. It is noted that the main amplifier's power has the largest contribution to power production.

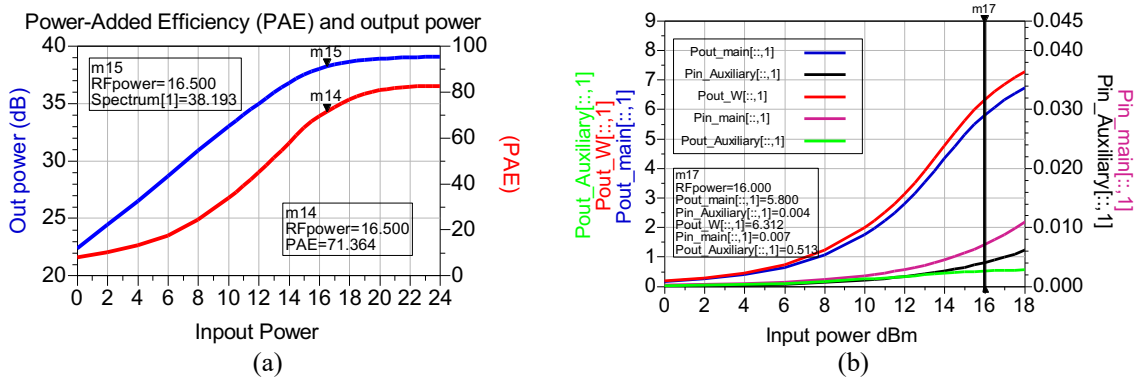


Fig. 8. Results of the single-tone test: (a) The relation between output power and PAE in regard to variations in input power: (b) Power distribution between the carrier and peaking amplifiers

Fig. 9 shows that the amplifier has a high attenuation factor for unwanted components and this is very clear from comparing the power of the original component to the power of the third harmonic component. The latter component's power is 44 dB lower than the fundamental component's power. This result shows that the power ratio of the third component to the first component is very low, indicating that unwanted components are attenuated. In addition, the fundamental component's power response does not intersect with the third harmonic component's power response, indicating that the intersection points are far apart, another indication of the amplifier's high linearity [46], [47].

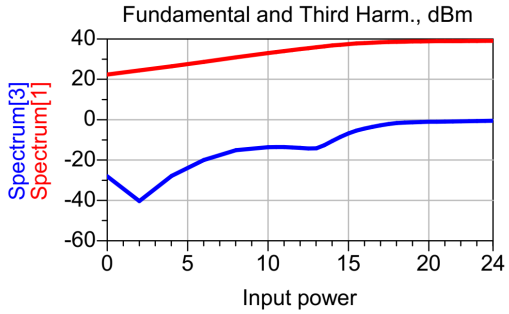


Fig. 9. fundamental and third harmonic component response

Furthermore, through a single-tone simulation, we can study and analyze the proposed amplifier's output impedance (RL) and how it interacts with changes in the output impedances of both the main and auxiliary amplifiers as power changes. This analysis indicates that the power distribution method in the symmetrical amplifier increases the efficiency of the load modulation network in maintaining a constant output impedance (RL) despite changes in the main and auxiliary amplifier impedances. This, in turn, explains the improved linearity of the proposed power amplifier [48]–[50]. Fig. 10 illustrates the results of this analysis.

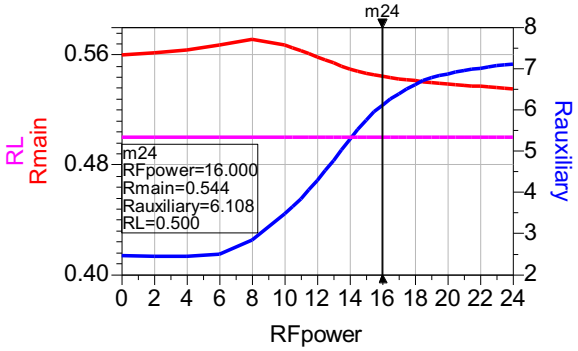
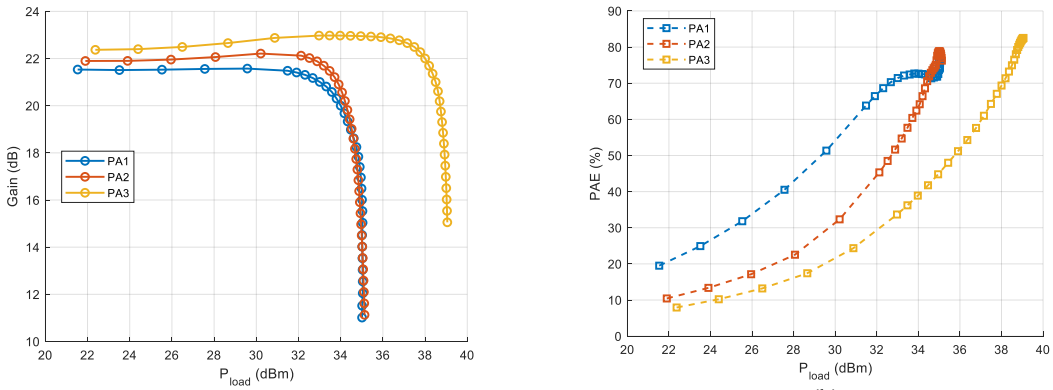


Fig. 10. The output impedance of the main and auxiliary amplifiers is compared with the output impedance of the load modulation network as a function of the input power

The results from the single-tone test for the basic amplifiers (PA1) and (PA2) were compared to the final design results of the modified Doherty power amplifier (PA3). The results obtained are shown in Table 1 and Fig. 11. It was found that the proposed amplifier in its final form achieved a high output power of 38 dBm with a difference of 4-5 dB compared to the other amplifiers. This indicates the effectiveness of the proposed technology in power amplification. Another important indicator is maintaining the linearity of the amplifier over a wide dynamic range of up to 12 dB. This fact is shown by comparing the performance of the three amplifiers in Table 1 through the values of third-order harmonic distortion (THD dBc) and the values of phase and amplitude distortion with varying power. The above results clearly demonstrate that the added power efficiency (PAE) and gain fluctuate as the output power changes. The efficiency of PA3 was found to be lower than that of PA1. This variance is due to the presence of amplifiers connected in parallel in the case of PA3. These amplifiers require a bias current that is double that of the other amplifiers. However, this issue does not appear significantly at high power levels, but it starts to emerge after a power drop of 8 dBm. Efficiency decreases with the decline in power until we reach the end of the amplifier's dynamic range. Thus, through the Figure of Merit, the proposed amplifier can be considered suitable for modern communication system applications [51], [52].

Table 1. Comparison of the characteristics of the final proposed amplifier PA 3 with the characteristics of the basic amplifiers PA 1 and PA 2

	Gain dB	PAE @pmax	PAE @-6 dB	Pout max dBm	DR dBm	THD dBc	AM/AM dB/dB	AM/PM degrees/dB	Topology of Power amplifier	FOM %
PA1	21	72	40	33	12	-40	(0.4)-(1) 0.6	(-1)-(0) 1	Doherty	70
PA2	22	60	21	34	10	-42	(0.3)-(1.1) 0.8	(-0.2)-(1) 1.2	Symmetrical Doherty	72
PA3	23	71	30	38	12	-44	(0.4)-(1.1) 0.7	(-1)-(1) 2	Modified Doherty (MDPA)	82



(a) (b)

Fig. 11. Performance of the three-stage amplifier as a function of output power changes: (a) power Added efficiency PAE: (b) Power gain

4.3. Sensitivity of the Amplifier

The main purpose of this design is to prove the effectiveness of the modulated Doherty amplifier (MDPA) technique. To enhance the simulation results, the sensitivity of the amplifier to changes in the influencing amplifier elements was tested by testing the amplifier characteristics when the gate voltage (VGS) and the characteristic impedance of the transmission line (TL3) change by ±10%. Table 2 shows the scenario followed for changing the circuit component values and the results obtained from this change.

Table 2. The procedure undertaken to modify the circuit component values and what outcomes from this alteration

Variables			Results		
Characteristic impedance Z0 TL2	**VGS**	**Gain**	**Output power**	**PAE**	**THD**
45	-2.16	Gain1	Po1	PAE1	THD1
47.5	-2.2	Gain2	Po2	PAE2	THD2
50	-2.4	Gain3	Po3	PAE3	THD3
52.5	-2.52	Gain4	P4	PAE4	THD4
55	-2.64	Gain5	P5	PAE5	THD5

Fig. 12 shows that the sensitivity of the proposed amplifier is acceptable to changes in the bias voltage, as shown by the gain, output power, and efficiency results. However, the sensitivity is very significant when the voltage drops to -2.64, as shown by the clear deterioration of these values. This decrease is due to the fact that switched amplifiers are very sensitive to changes in bias [53]–[55]. As for the THD value, the change is slight and insignificant. Fig. 13 shows that changing the characteristic impedance value of the line (TL3) has a slight effect, indicating that the amplifier's characteristics are negligibly affected by this element. This test demonstrates the varying sensitivity of the amplifier to changes in the values of its main components, which provides a clear impression through which it is possible to determine the acceptable limits for changing component values and determine the operating conditions.

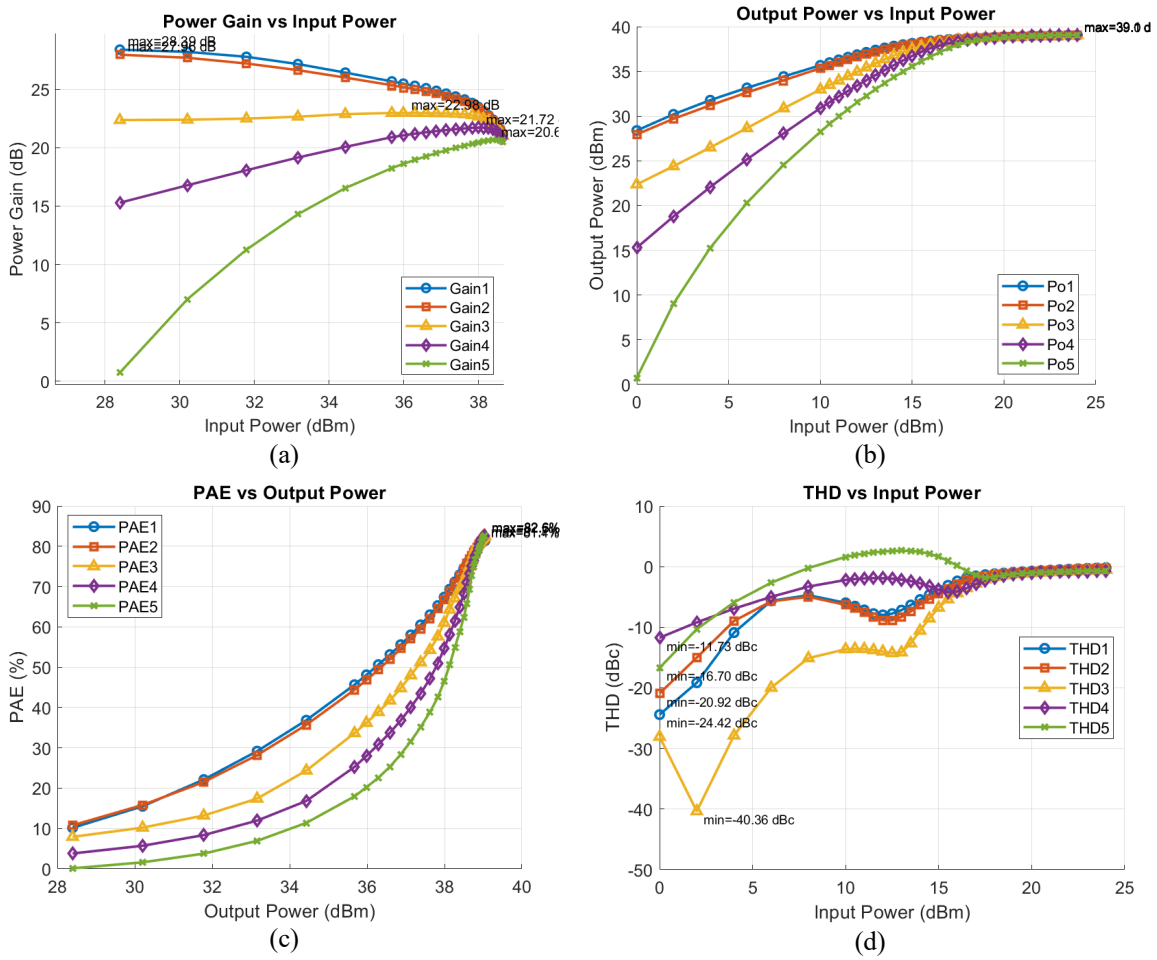


Fig. 12. The impact of variations in the VGS value on the amplifier's principal performance parameters: (a)Gain; (b) Output power; (c) PAE; and (d) THD

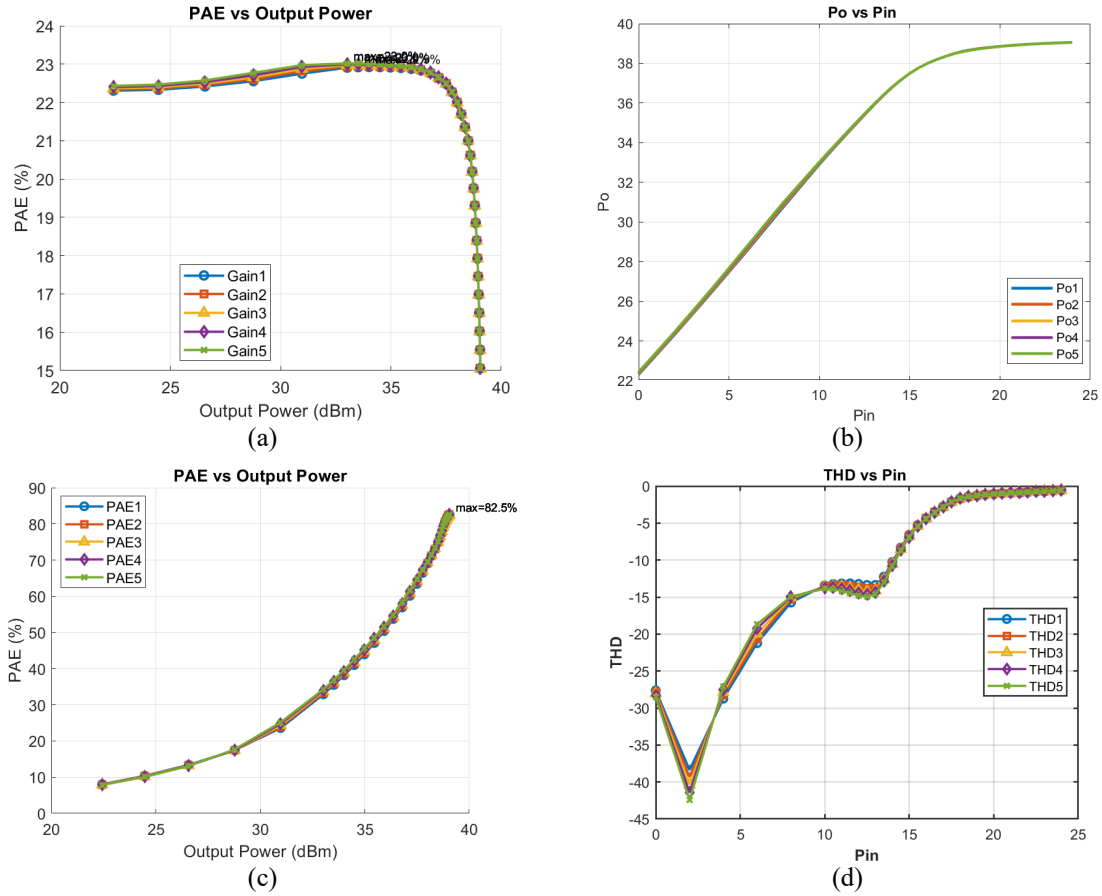


Fig. 13. The impact of variations in the Z0 TL2 value on the amplifier's parameters: (a) Gain; (b) Output power; (c) PAE; and (d) THD

4.4. Two-Tone Harmonic Balance

Two-tone analysis is employed to illustrate distortion in nonlinear circuits when two signals are concurrently input, resulting in interference. This study enables the assessment of power amplifier properties, namely gain, power-added efficiency, and intermodulation distortion (IMD) [56]. The designed amplifier was tested with a two-tone signal with a mean frequency of 850 MHz and a bandwidth varying from 20 to 150 MHz. The amplifier demonstrated satisfactory response up to a bandwidth of 100 MHz, achieving an output power of 29.5 dBm, a gain of 17 dB, and a PAE of 30% (See Fig. 14).

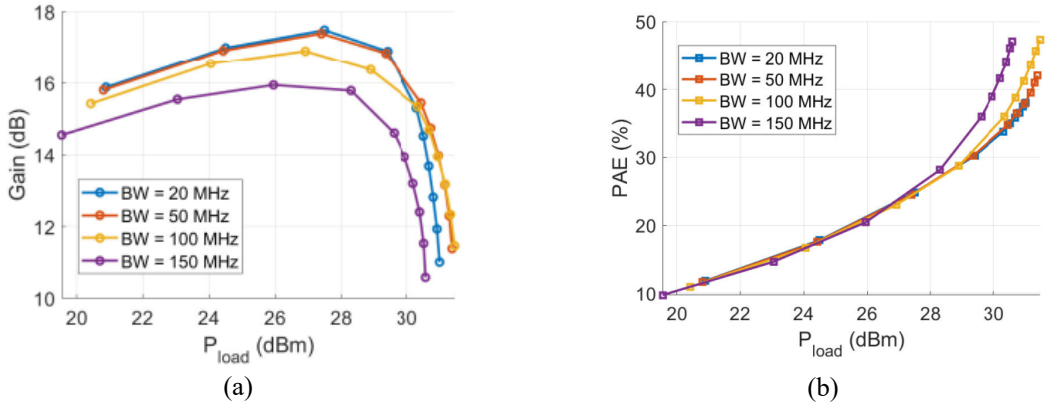


Fig. 14. The amplifier characteristics change with varying bandwidths for different output power values. (a) Power gain, (b) Power-added efficiency

The proposed amplifier's linearity performance at a bandwidth of 100 MHz was assessed by measuring the third-order intermodulation distortion (IMD) value produced by a two-tone signal within the same bandwidth. The third-order IMD value was less than 18 dBc at maximum output power. Fig. 15 illustrates the spectrum of the two-tone signal and the variation in the IMD value as a function of output power changes under these conditions.

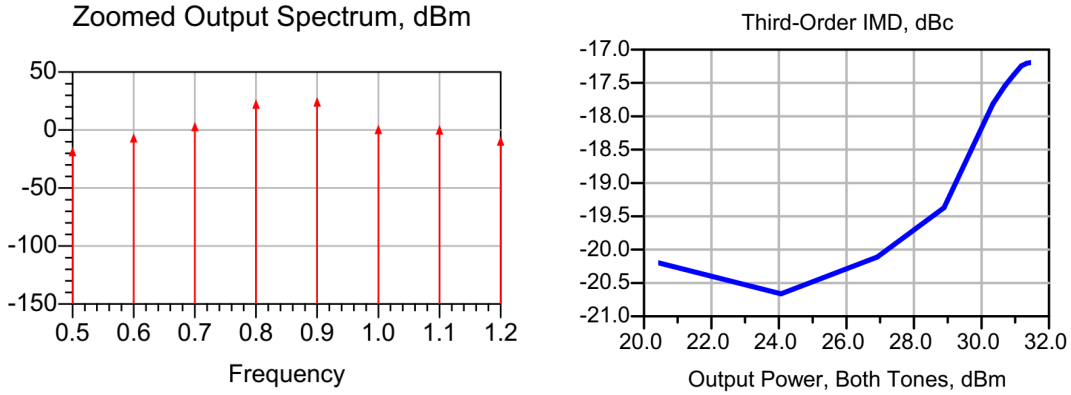


Fig. 15. Amplifier response to a two-tone signal: (a) Output spectrum; (b) Third-order IMD

A multitude of scholars have investigated the design of power amplifiers for modern communication systems to enhance output power and efficiency using several techniques. Table 3 juxtaposes the outcomes of the suggested amplifier with those from prior research. These investigations demonstrate that a trade-off between efficiency and output power is unavoidable owing to the nonlinear characteristics of the power amplifier [48], [57]–[59]. This is easily demonstrated by juxtaposing the outcomes of the suggested design with prior results. Although the suggested amplifier (MDPA) did not surpass [16] and [52] in output power, its superiority was unequivocally proved in terms of efficiency, linearity, and dynamic range (DR). Consequently, the outcomes derived from the modified Doherty power amplifier (MDPA) has characteristics that render it appropriate for various applications.

Table 3. Comparison of the suggested amplifier's results with those of prior studies

Properties	2023 [1]	2021 [15]	2021 [16]	2021 [52]	2023 [60]	This Work
Frequency (GHz)	0.85	0.91	1.68	3.3	3.3	0.85
Pout (dBm)	22.7	33.8	43.5	45	45	38
Gain (dB)	12	34.6	13.5	11.4	12	23
PAE%	60	54.5	53.6	70.1	56	71.3
DR (dB)	7.3	7.8	9.6	9	7.5	12
Bw (MHz)	100	10	10	60	500	100
Technique	Inverted Doherty	IMD3 Cancellation Method	Doherty	Load Modulated	Modulated Balanced	Modified Doherty (MDPA)
Application	Power-Combining	Power-Combining	Complex Combining Load	Efficiency Enhancement	Power Amplifier	Power Combiner

5. Conclusion

In this study, a modified Doherty power amplifier (MDPA) model was proposed to achieve a high performance in terms of efficiency, linearity, and output power. The main and auxiliary amplifiers are constructed using two identical amplifiers with the same bias point. The E-type switching amplifier served as the basic model for building the two amplifiers. The current gain of the main amplifier was doubled by connecting two amplifiers in parallel, while voltage amplification was

emphasized in the auxiliary amplifier. The optimization principle for distributing power between the main and auxiliary amplifiers was implemented by controlling the input impedance of both amps. The ADS simulation program was used to implement and test the proposed amplifier. The simulation results proved that the use of a switching amplifier is effective in enhancing the amplifier's efficiency. Simultaneous voltage and current amplification significantly increased the amplifier's gain and output power. The asymmetric power distribution and the load modulation network enhanced the amplifier's dynamic range and bandwidth by achieving optimal matching, which involved maintaining the amplifier's output impedance and minimizing the impact of parasitic components as power levels change. The designed model was tested with a single-tone signal at 850 MHz. The amplifier demonstrated a power-added efficiency (PAE) of 71.3% at an output power of 38 dBm and a dynamic range of 12 dB. Based on the obtained results and comparison with previous works, the proposed amplifier is a suitable option for modern communication systems and can be practically implemented.

Author Contribution: All authors contributed equally to the main contributor to this paper. All authors read and approved the final paper.

Acknowledgment: The authors extend their deep appreciation to the University of Mosul, College of Engineering, Department of Electrical Engineering for their vital assistance in the fulfillment of this work.

Conflicts of Interest: The authors declare no conflict of interest.

References

[1] G. D. Singh, H. M. Nemati, M. S. Alavi, and L. C. N. de Vreede, "An inverted Doherty power amplifier insensitive to load variation with an embedded impedance sensor in its output power-combining network," *IEEE Transactions on Microwave Theory and Techniques*, vol. 71, no. 12, pp. 5194–5208, 2023, https://doi.org/10.1109/TMTT.2023.3277081.

[2] M. Li, J. Pang, Y. Li, and A. Zhu, "Bandwidth enhancement of Doherty power amplifier using modified load modulation network," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 6, pp. 1824–1834, 2020, https://doi.org/10.1109/TCSI.2020.2972163.

[3] J. Pang, C. Chu, Y. Li, and A. Zhu, "Broadband RF-input continuous-mode load-modulated balanced power amplifier with input phase adjustment," *IEEE Transactions on Microwave Theory and Techniques*, vol. 68, no. 10, pp. 4466–4478, 2020, https://doi.org/10.1109/TMTT.2020.3012141.

[4] S. Verploegh, T. Sonnenberg, M. Pinto, A. Babenko, and Z. Popović, "On-chip power combining with 3-stage 75–110 GHz GaN MMIC power amplifiers," in *Proceedings of the 51st European Microwave Conference*, 2021, pp. 890–893, https://doi.org/10.23919/EuMC50147.2022.9784324.

[5] A. S. Al-Jawadi, M. T. Yaseen, and Q. T. Algwari, "Gate engineering solutions to mitigate short channel effects in a 20 nm MOSFET," *e-Prime – Advances in Electrical Engineering, Electronics and Energy*, vol. 11, p. 100934, 2025, https://doi.org/10.1016/j.prime.2025.100934.

[6] A. S. Al-Jawadi, M. T. Yaseen, and Q. T. Algwari, "TCAD-based analysis of a novel dual dielectric gate MOSFET for high-speed applications," *Silicon*, vol. 17, pp. 2921–2932, 2025, https://doi.org/10.1007/s12633-025-03386-5.

[7] M. N. Zahid, F. Javeed, and G. Zhu, "Design analysis of advanced power amplifiers for 5G wireless applications: A survey," *Analog Integrated Circuits and Signal Processing*, vol. 118, no. 2, pp. 199–217, 2024, https://doi.org/10.1007/s10470-023-02193-5.

[8] S. Elkhaldi, M. El Bakkali, N. A. Touhami, T. Elhamadi, and H. Abdelmounim, "Linearization, EM simulation, and realization of a 40 dBm class-AB GaN power amplifier," *International Journal of Electrical and Electronics Research*, vol. 12, no. 4, pp. 1418–1426, 2024, https://doi.org/10.37391/ijeer.120436.

[9] C. Ramella, M. Pirola, C. Florian, and P. Colantonio, "Space-compliant design of a millimeter-wave GaN-on-Si stacked power amplifier cell through electromagnetic and thermal simulations," *Electronics*, vol. 10, no. 15, p. 1784, 2021, https://doi.org/10.3390/electronics10151784.

[10] F. Costanzo, V. Camarchia, N. B. Carvalho, P. Colantonio, A. Piacibello, R. Quaglia, V. Valenta, and R. Giofrè, "A GaN MMIC stacked Doherty power amplifier for space applications," in *Proceedings of the 2022 IEEE Topical Conference on RF/Microwave Power Amplifiers for Radio and Wireless Applications (PAWR)*, 2022, pp. 29–31, https://doi.org/10.1109/PAWR53092.2022.9719789.

[11] S. Veisee, R. Liu, and A. Zhu, "An efficiency-enhanced GaN MMIC nonuniform distributed power amplifier using a modified gate line structure," *IEEE Transactions on Microwave Theory and Techniques*, vol. 73, no. 6, pp. 3503–3513, 2025, https://doi.org/10.1109/TMTT.2024.3499753.

[12] Shailesh, G. Srivastava, and S. Kumar, "A state-of-the-art review on distributed amplifiers," *Wireless Personal Communications*, vol. 117, pp. 1471–1525, 2021, https://doi.org/10.1007/s11277-020-07932-9.

[13] J. Kim and Y. Sung, "Triple-stacked FET distributed power amplifier using 28 nm CMOS process," *Electronics*, vol. 13, no. 22, p. 4433, 2024, https://doi.org/10.3390/electronics13224433.

[14] V. Camarchia, R. Quaglia, A. Piacibello, D. P. Nguyen, H. Wang, and A.-V. Pham, "A review of technologies and design techniques of millimeter-wave power amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 68, no. 7, pp. 2957–2983, 2020, https://doi.org/10.1109/TMTT.2020.2989792.

[15] K. Oh, H. Ahn, I. Nam, H. D. Lee, B. Park, and O. Lee, "A dual-mode InGaP/GaAs HBT power amplifier using a low-loss parallel power-combining transformer with IMD3 cancellation method," *Electronics*, vol. 10, no. 14, p. 1612, 2021, https://doi.org/10.3390/electronics10141612.

[16] W. Choi, H. Kang, H. Oh, K. C. Hwang, K.-Y. Lee, and Y. Yang, "Doherty power amplifier based on asymmetric cells with complex combining load," *IEEE Transactions on Microwave Theory and Techniques*, vol. 69, no. 4, pp. 2336–2344, 2021, https://doi.org/10.1109/TMTT.2021.3059666.

[17] J. Pang, C. Chu, J. Wu, Z. Dai, M. Li, S. He, and A. Zhu, "Broadband GaN MMIC Doherty power amplifier using continuous-mode combining for 5G sub-6 GHz applications," *IEEE Journal of Solid-State Circuits*, vol. 57, no. 7, pp. 2143–2154, 2022, https://doi.org/10.1109/JSSC.2022.3145349.

[18] S. Makhsuci, S. M. Navidi, M. Sanduleanu, and M. Ismail, "A review of Doherty power amplifier and load modulated balanced amplifier for 5G technology," *International Journal of Circuit Theory and Applications*, vol. 51, no. 5, pp. 2422–2445, 2023, https://doi.org/10.1002/cta.3521.

[19] N. S. Mannem, T.-Y. Huang, and H. Wang, "Broadband active load-modulation power amplification using coupled-line baluns: A multifrequency role-exchange coupler Doherty amplifier architecture," *IEEE Journal of Solid-State Circuits*, vol. 56, no. 10, pp. 3109–3122, 2021, https://doi.org/10.1109/JSSC.2021.3078322.

[20] G. Nikandish, R. B. Staszewski, and A. Zhu, "Breaking the bandwidth limit: A review of broadband Doherty power amplifier design for 5G," *IEEE Microwave Magazine*, vol. 21, no. 4, pp. 57–75, 2020, https://doi.org/10.1109/MMM.2019.2963607.

[21] V. Vorapipat, C. S. Levy, and P. M. Asbeck, "A class-G voltage-mode Doherty power amplifier," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 12, pp. 3348–3360, 2017, https://doi.org/10.1109/JSSC.2017.2748283.

[22] Y. Zhang, R. Gao, S. Liu, Y. Han, M. Ren, H. Lin, and J. Pang, "Analysis and design of symmetrical coupled Doherty power amplifier with extended high-efficiency range," *AEU – International Journal of Electronics and Communications*, vol. 187, p. 155509, 2024, https://doi.org/10.1016/j.aeue.2024.155509.

[23] Y. Xu, J. Pang, X. Wang, and A. Zhu, "Enhancing bandwidth and back-off range of Doherty power amplifier with modified load modulation network," *IEEE Transactions on Microwave Theory and Techniques*, vol. 69, no. 4, pp. 2291–2303, 2021, https://doi.org/10.1109/TMTT.2021.3056402.

[24] A. Piacibello, V. Camarchia, P. Colantonio, and R. Giofrè, "3-way Doherty power amplifiers: Design guidelines and MMIC implementation at 28 GHz," *IEEE Transactions on Microwave Theory and Techniques*, vol. 71, no. 5, pp. 2016–2028, 2022, https://doi.org/10.1109/TMTT.2022.3225316.

[25] H. Zhou, V. Åberg, H. Chang, and C. Fager, "A GaN MMIC wideband continuous-mode Doherty power amplifier for 6G FR3 cmWave applications," in *Proceedings of the 19th European Microwave Integrated Circuits Conference (EuMIC)*, 2024, pp. 170–173, https://doi.org/10.23919/EuMIC61603.2024.10732713.

[26] H. Choi, "A Doherty power amplifier for ultrasound instrumentation," *Sensors*, vol. 23, no. 5, p. 2406, 2023, https://doi.org/10.3390/s23052406.

[27] S. Alemdar and A. Atalar, "Doherty power amplifier output networks with maximized bandwidth," *International Journal of Microwave and Wireless Technologies*, vol. 15, no. 3, pp. 393–409, 2023, https://doi.org/10.1017/S1759078722000381.

[28] A. Nasri, M. Estebsari, S. Toofan, A. Piacibello, M. Pirola, V. Camarchia, and C. Ramella, "Broadband class-J GaN Doherty power amplifier," *Electronics*, vol. 11, no. 4, p. 552, 2022, https://doi.org/10.3390/electronics11040552.

[29] A. A. Ismael, A. T. Younis, E. A. Abdo, and S. H. Hussein, "Improvement of non-linear power amplifier performance using Doherty technique," *Journal of Engineering Science and Technology*, vol. 16, no. 6, pp. 4481–4493, 2021, https://jestec.taylors.edu.my/Vol 16 Issue 6 December 2021/16_6_9.pdf.

[30] A. A. Ismael and M. T. Yaseen, "Design and implementation of a high-performance 850 MHz class-E power amplifier for 5G NR applications," *Instrumentation, Measurement and Metrology*, vol. 24, no. 1, p. 81, 2025, https://doi.org/10.18280/i2m.240109.

[31] Q. Lin, L. Jia, H. Wu, and X. Wang, "Investigation on temperature behavior for a GaAs E-pHEMT MMIC LNA," *Micromachines*, vol. 13, no. 7, p. 1121, 2022, https://doi.org/10.3390/mi13071121.

[32] W. Chen, Y. Wu, S. Li, and W. Wang, "Fully integrated broadband GaAs MMIC load modulated balanced amplifier for sub-6 GHz applications," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 70, no. 8, pp. 2834–2838, 2023, https://doi.org/10.1109/TCSII.2023.3246042.

[33] K. Xie, K. Wang, and H. Zhang, "A two-way three-stage W-band power amplifier with series-parallel inductor-based T-type inter-stage matching network," *Microelectronics Journal*, vol. 135, p. 105770, 2023, https://doi.org/10.1016/j.mejo.2023.105770.

[34] H. Lu, M. Zhang, L. Yang, B. Hou, R. Perez Martinez, M. Mi, J. Du, L. Deng, M. Wu, S. Chowdhury, X. Ma, and Y. Hao, "A review of GaN RF devices and power amplifiers for 5G communication applications," *Fundamental Research*, vol. 5, no. 1, pp. 315–331, 2025, https://doi.org/10.1016/j.fmre.2023.11.005.

[35] H. Zhao, J. Liu, T. Rong, S. Fan, Z. Chen, and J. Wang, "Modeling of multi-cell HBT device based on device structure," *Micromachines*, vol. 16, no. 4, p. 433, 2025, https://doi.org/10.3390/mi16040433.

[36] D. Zhao, H. Wang, Y. Chen, S. Wang, J. Shao, Z. Fu, and S. Duan, "An 8-way series-parallel combiner based power amplifier for mm-wave 5G communication in 40-nm CMOS," *AEU – International Journal of Electronics and Communications*, vol. 177, p. 155238, 2024, https://doi.org/10.1016/j.aeue.2024.155238.

[37] H. Li, S. Zhao, X. Wang, L. Ding, and H. A. Mantooth, "Parallel connection of silicon carbide MOSFETs—Challenges, mechanism, and solutions," *IEEE Transactions on Power Electronics*, vol. 38, no. 8, pp. 9731–9749, 2023, https://doi.org/10.1109/TPEL.2023.3278270.

[38] B. Rautio and T. Barton, "A study on GaN MMIC power amplifier stability–performance design tradeoffs at X band," in *Proceedings of the IEEE Wireless and Microwave Technology Conference (WAMICON)*, 2025, pp. 1–4, https://doi.org/10.1109/WAMICON64429.2025.11004121.

[39] M. Kojourimanesh, V. Kornilov, I. Lopez Arteaga, and P. de Goey, "Stability criteria of two-port networks, application to thermo-acoustic systems," *International Journal of Spray and Combustion Dynamics*, vol. 14, no. 1–2, pp. 82–97, 2022, https://doi.org/10.1177/17568277221088465.

[40] J. Wang, C. Wang, S. Zhao, H. Li, L. Ding, X. Shen, and H. A. Mantooth, "Comprehensive analysis of paralleled SiC MOSFETs current imbalance under asynchronous gate signals," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 11, no. 5, pp. 4850–4866, 2023, https://doi.org/10.1109/JESTPE.2023.3290935.

[41] T.-C. Tsai and A. Ć. Ulusoy, "A SiGe common-collector-common-base linear power amplifier with 17-28-GHz P 1 dB 3-dB bandwidth and enhanced large-signal stability," in *2025 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2025, pp. 287-290. https://doi.org/10.1109/RFIC61188.2025.11082791.

[42] A. Mateo, I. Lizarraga, J. Terrer, A. Anakabe, and J. M. Collantes, "Unconditional stability analysis of N-port networks based on structured singular value computation," in *2024 IEEE Asia-Pacific Microwave Conference (APMC)*, 2024, pp. 1275-1277. https://doi.org/10.1109/APMC60911.2024.10867452.

[43] H. F. Ganji, V. Kornilov, J. van Oijen, I. Lopez Arteaga, and P. de Goey, "Discussing the limitations of unconditional stability indicators in evaluating thermoacoustic quality of burners with flames," *International Journal of Spray and Combustion Dynamics*, vol. 16, no. 4, pp. 231-246, 2024. https://doi.org/10.1177/17568277241265433.

[44] X. Wang, Z. Li, and T. Xu, "A sub-6GHz wideband low noise amplifier with high gain and low noise figure in 110-nm SOI CMOS," *Electronics Letters*, vol. 59, no. 17, p. e12942, 2023. https://doi.org/10.1049/ell2.12942.

[45] M.-S. Kim and S.-S. Yoo, "RF-SOI low-noise amplifier using RC feedback and series inductive-peaking techniques for 5G new radio application," *Sensors*, vol. 23, no. 13, p. 5808, 2023. https://doi.org/10.3390/s23135808.

[46] A. Borel, V. Barzdėnas, and A. Vasjanov, "Linearization as a solution for power amplifier imperfections: A review of methods," *Electronics*, vol. 10, no. 9, p. 1073, 2021. https://doi.org/10.3390/electronics10091073.

[47] H. Lyu, Y. Cao, and K. Chen, "Linearity-enhanced quasi-balanced Doherty power amplifier with mismatch resilience through series/parallel reconfiguration for massive MIMO," *IEEE Transactions on Microwave Theory and Techniques*, vol. 69, no. 4, pp. 2319-2335, 2021. https://doi.org/10.1109/TMTT.2021.3056488.

[48] Y. Jin, Z. Dai, X. Ran, C. Xu, and M. Li, "A dual load-modulated Doherty power amplifier design method for improving power back-off efficiency," *Sensors*, vol. 23, no. 14, p. 6598, 2023. https://doi.org/10.3390/s23146598.

[49] A. Atanaskovic, N. Males-Ilic, A. Djoric, and D. Budimir, "Doherty amplifier linearization by digital injection methods," *Facta Universitatis, Series: Electronics and Energetics*, vol. 35, no. 4, pp. 587-601, 2022. https://doi.org/10.1109/TELSIKS52058.2021.9606416.

[50] J. Guo, Y. Cao, and K. Chen, "Linear hybrid asymmetrical load-modulated balanced amplifier with multiband reconfigurability and antenna-VSWR resilience," *IEEE Transactions on Microwave Theory and Techniques*, vol. 72, no. 9, pp. 5319-5332, 2024. https://doi.org/10.1109/TMTT.2024.3381845.

[51] S. Bhardwaj and J. Kitchen, "Broadband parallel Doherty power amplifier in GaN for 5G applications," in *2019 IEEE Topical Conference on RF/Microwave Power Amplifiers for Radio and Wireless Applications (PAWR)*, 2019, pp. 1-3. https://doi.org/10.1109/PAWR.2019.8708727.

[52] Y. Xu, J. Pang, X. Wang, and A. Zhu, "Three-stage load modulated power amplifier with efficiency enhancement at power back-off," *IEEE Transactions on Microwave Theory and Techniques*, vol. 69, no. 6, pp. 3107-3119, 2021. https://doi.org/10.1109/TMTT.2021.3061436.

[53] S. Pezeshkpour and M. M. Ahmadi, "Design procedure for a high-efficiency class-E/F³ power amplifier," *IEEE Transactions on Power Electronics*, vol. 38, no. 11, pp. 14388-14399, 2023. https://doi.org/10.1109/TPEL.2023.3286731.

[54] Y. Komiyama, A. Komanaka, W. Zhu, A. Konishi, K. Nguyen, and H. Sekiya, "Analysis and design of load-independent series resonant power amplifier with constant current output and its application for WPT system," *IEEE Transactions on Power Electronics*, vol. 39, no. 5, pp. 6515-6525, 2024. https://doi.org/10.1109/TPEL.2024.3367373.

[55] A. V. Dolgopyatova and O. V. Varlamov, "Reverse intermodulation distortion in current mode and bridge class D RF power amplifiers," in *2023 Systems of Signals Generating and Processing in the Field of on Board Communications*, 2023, pp. 1-7. https://doi.org/10.1109/IEEECONF56737.2023.10092117.

[56] L. F. Gonçalves, T. Zhang, G. Raithel, and D. A. Anderson, "Non-linearities in atomic quantum receivers: Harmonic and intermodulation distortion," *arXiv Preprint*, arXiv:2412.16366, 2024. https://arxiv.org/abs/2412.16366.

[57] N. M. Laskar, K. Guha, S. Nath, S. Chanda, K. L. Baishnab, P. K. Paul, and K. S. Rao, "Design of high gain, high bandwidth neural amplifier IC considering noise-power trade-off," *Microsystem Technologies*, vol. 27, no. 2, pp. 585-599, 2021. https://doi.org/10.1007/s00542-018-4142-5.

[58] Z. Zhang, A. Piacibello, and V. Camarchia, "Efficiency versus linearity trade-off in an S-band class-AB power amplifier," in *2023 IEEE Topical Conference on RF/Microwave Power Amplifiers for Radio and Wireless Applications*, 2023, pp. 26-28. https://doi.org/10.1109/PAWR56957.2023.10046214.

[59] T. He, Y. Zheng, X. Liang, J. Li, L. Lin, W. Zhao, Y. Li, and J. Zhao, "A highly energy-efficient body-coupled transceiver employing a power-on-demand amplifier," *Cyborg and Bionic Systems*, vol. 4, p. 30, 2023. https://doi.org/10.34133/cbsystems.0030.

[60] S. E. Mochumbe and Y. Yang, "Design of a load modulated balanced amplifier with a two-stage control power amplifier," *Journal of Electromagnetic Engineering and Science*, vol. 23, no. 3, pp. 294-301, 2023. https://doi.org/10.26866/jees.2023.3.r.170.