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A Single-Phase Boost Switched-Capacitor Seven-Level Inverter With Eight Switches

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ABSTRACT

This paper proposes a seven-level boost switched-capacitor inverter utilizing only eight active switches (8S7L-BSCI). The study addresses several limitations of conventional SC-MLI configurations, which often require multiple DC sources, lack inherent capacitor voltage balancing, or involve a high semiconductor count leading to increased switching losses. To overcome these challenges, the 8S7L-BSCI integrates a two-stage switched-capacitor (SC) network with a full H-bridge, enabling triple voltage boosting and seven-level output generation without additional DC sources, transformers, or front-end boost converters. The objective of this work is to develop a single-source inverter with high voltage gain, intrinsic capacitor-voltage balancing, and reduced device voltage stress. As a result, the proposed inverter is well suited for low-voltage PV systems and energy-storage applications. The main contribution lies in proposing a simplified SC-MLI architecture in which only two MOSFETs operate at high frequency while the remaining switches function at the line frequency, thereby reducing switching losses and control complexity. The paper presents a detailed explanation of the operating principles of the two-stage SC network, the Boolean-logic-based PWM strategy, and comparative evaluations with existing topologies. Simulation and experimental results from a hardware prototype of approximately 330 W confirm the feasibility of the proposed inverter, demonstrating stable operation with an efficiency of about 95% ± 1.3%. Furthermore, the inverter delivers high-quality output with harmonic distortion maintained below 1% under inductive loading conditions.

1. Introduction

Recently, the rapid growth of renewable-energy systems and high-power electric drives has imposed increasingly stringent requirements on power converters, including higher conversion efficiency, superior output-voltage quality, lower losses, and simpler hardware structures. Against this backdrop, the multilevel inverter (MLI) has emerged as a promising solution for high-quality DC-to-AC power conversion [1]-[4]. Conventional topologies Neutral-Point-Clamped (NPC) [5]-[13], Flying-Capacitor (FC) [14], [15], Cascaded H-Bridge (CHB) [16]-[20], and T-type converters

have been widely adopted because they distribute the blocking voltage across individual switches and significantly improve the output waveform quality [22]-[27]. However, in low-input-voltage applications such as photovoltaic (PV) systems, these topologies exhibit significant drawbacks: they lack intrinsic voltage-boost capability, require a large number of power devices, suffer from challenging capacitor-voltage balancing, and demand complex control schemes [12]-[14], [26]-[32].

In systems powered by low-voltage DC sources such as photovoltaic (PV) arrays or electric-vehicle battery packs, a voltage-boost function is indispensable to reach the required AC output level. One practicable solution is to cascade a standalone DC-DC boost converter with a two-stage multilevel inverter; however, this approach inevitably raises the semiconductor switch count, exacerbates switching losses, and complicates the overall control architecture [33]-[37]. Moreover, the CHB topology necessitates multiple isolated DC sources [37], [38]; this requirement is difficult to satisfy in stand-alone PV systems, where only a single low-voltage source is available [39]-[44].

To overcome these limitations, recently, considerable research has been directed toward single-stage boost multilevel inverters that employ switched-capacitor (SC) topology [40]-[53]. These topologies synthesize positive voltage levels by orchestrating specific capacitor charge-discharge sequences and are subsequently combined with H-bridge stages or polarity-inversion circuits to produce the AC output voltage. Several prominent studies such as [30]-[35], [40]-[51] demonstrate that switched-capacitor multilevel inverters can realize voltage-boost factors of 2-4 and generate between five and nine distinct output levels, using only a single DC source and no inductors. However, several challenges remain unresolved:

- A high power-switch count (≥ 9 switches for five voltage levels as in [21], [28], [34], or 9–12 switches for seven voltage levels as in [40]-[51], and nine to thirteen voltage levels as in [42]-[44] which increases cost and control complexity.
- High voltage stress on the switch can reach up to 2-3 times the input voltage V_{DC}, as in [30]-[35], [40]-[42], [47]-[49], which complicates the design process and makes the selection of appropriate semiconductor devices more difficult.
- Capacitor voltage balancing is challenging: certain topologies require voltage sensors or complex modulation techniques to achieve voltage balancing.
- Several existing switched-capacitor topologies do not effectively support inductive loads or high inrush currents when capacitors are connected in parallel [50]-[55].

Some notable advancements in recent switched-capacitor inverter topologies include the adoption of hybrid SPWM techniques to enhance waveform quality, optimizing the switching strategy to reduce losses [56]-[60], or reducing the number of capacitors to save space and hardware cost [3]-[5], [40]-[51]. However, no existing topology has yet achieved all the key objectives simultaneously, including a high voltage boosting gain, minimal number of switches, low voltage stress across switches, inherent capacitor voltage self-balancing without the need for voltage sensors, and a simple, easily implementable control strategy. To address these limitations, this paper proposes a novel topology called the Single-Phase Seven-Level Boost Switched-Capacitor Inverter employing eight power switches, abbreviated as 8S7L-BSCI, as shown in Fig. 1. This topology provides several advantages, including simultaneously achieving triple voltage boosting, seven-level voltage generation, and inherent capacitor self-balancing without sensors, using only eight semiconductor switches and three diodes. The design attains a very low switch-per-level ratio, significantly reduces switching losses since only two MOSFETs operate at high frequency, and lowers voltage stress on the devices while maintaining high efficiency. These features provide a compact, high-performance, and cost-effective solution compared with many existing SC-MLI structures, making it particularly suitable for low-voltage PV systems and energy-storage applications. More specifically, the topology consists of two main stages: The switched-capacitor stage consists of switches S_1 to S_4 and capacitors C_1, C_2 and C_{CD}. It performs the charging and discharging of capacitors in series to generate three corresponding positive voltage levels, V_{DC}, $2V_{DC}$ and $3V_{DC}$; and the output inverter stage with a full H-bridge configuration is responsible for generating a symmetrical seven-level AC voltage. The

proposed topology operates based on a time-phased switching principle with symmetrical state design, which inherently maintains capacitor voltage balance without requiring any voltage sensors or additional control algorithms for voltage compensation. A notable feature of the proposed topology is the optimized distribution of voltage stress. The high-frequency switches S_1-S_2 withstand only V_{DC}, while S_3-S_4 experience up to $2V_{DC}$ depending on the capacitor charging state. The H-bridge switches S_5-S_8 withstand the full output voltage of $3V_{DC}$. This arrangement allows the use of low-voltage MOSFETs in the boost stage and requires high-voltage devices only in the polarity-reversal stage, helping reduce losses and overall cost. As a result of these design enhancements, the proposed 8S7L-BSCI topology successfully realizes multiple performance advantages concurrently: The voltage-boosting gain reaches up to three times without the use of inductors, and the total number of power switches is limited to eight, which is fewer than the number used in the topologies employing nine or more switches, as reported in [41]-[48]. The capacitor voltages are self-balanced through the intrinsic charge–discharge mechanism, eliminating the need for additional sensors or control actions. Experimental results show that the inverter operates stably under RL loading with significant inductive characteristics, where the power factor is less than unity and a clear phase lag exists between voltage and current. This condition typically disrupts the charge-discharge sequence in conventional switched-capacitor structures. Nevertheless, the output waveform maintains seven symmetrical voltage levels, and the capacitor voltages remain stable, thereby demonstrating effective support for inductive loads with low inrush current and continuous, stable output.

This paper addresses the aforementioned research gap by proposing an eight-switch seven-level boost switched-capacitor inverter (8S7L-BSCI) that achieves triple voltage boosting, generates seven output levels, and inherently balances capacitor voltages without sensors. The research hypothesis is that, through a symmetrically arranged switching sequence combined with a multicarrier PWM modulation strategy, the topology can maintain stable capacitor voltages while reducing switching losses.

This paper follows a systematic structure, including the introduction and analysis of related studies on multilevel inverter topologies and modulation techniques in Section 1. Section 2 presents the operating principle of the 8S7L-BSCI configuration and describes the PWM modulation method. Section 3 presents a comparison with other structures. Section 4 provides the simulation and experimental results, and Section 5 concludes the study and highlights its potential applications.

2. The Proposed Seven-Level Boost Switched-Capacitor Inverter Configuration Using Eight Power Switches (8S7L-BSCI)

2.1. Operating State of 8S7L-BSCI

The structure of the single-phase seven-level boost inverter is based on the switched-capacitor configuration with eight power switches in Fig. 1. The input source is a low direct current voltage V_{DC} from the PV module consisting of a multilevel boost circuit using switches S_1 and S_2 operating at high frequency, capable of generating seven output voltage levels, together with clamping diodes D_1 to D_3 that support flexible control of the capacitor charging and discharging process, and two switched capacitors, C_1 and C_2, that charge and discharge sequentially. Capacitor C_{CD} plays the role of stabilizing the DC bus voltage. The full H-bridge configuration is formed by four switches, S_5 to S_8, allowing the generation of a sinusoidal output AC voltage by reversing the voltage from the intermediate point connected to the boost stage. These switches usually operate at low frequency, serving to create both positive and negative polarities, thereby synthesizing the output waveform with multiple voltage levels. The maximum reverse voltage V_s of each switch is referenced to the DC voltage V_{DC}; using eight switches, the device blocking voltages of switches S_1 to S_8 (V_{si} with i = 1 to 8) are as follows:

$$V_{S1} = V_{S2} = V_{DC}; \frac{1}{2}V_{S3} = \frac{1}{2}V_{S4} = V_{DC}; \frac{1}{3} \times V_{S5} = \frac{1}{3} \times V_{S6} = \frac{1}{3} \times V_{S7} = \frac{1}{3} \times V_{S8} = V_{DC}; V_{dj} = V_{DC}; \quad (1)$$

Specifically, switch S_1 and diode D_1 together with floating capacitor C_1 form the first switched-capacitor stage, while S_2, D_2, and capacitor C_2 form the second switched-capacitor stage. Diode D_3 assists in directing the current during the charging process of C_2. Switches S_3 and S_4 are responsible for coordinating the synthesized voltage at low frequency after the switched-capacitor stages, before delivering this voltage to the full H-bridge S_5 to S_8, enabling extended modulation capability and control of the output voltage vector-allowing more flexible operation with PWM or Space Vector Modulation (SVM). At the same time, it also helps improve waveform quality and reduce harmonics. The output of the full H-bridge configuration is can be varied to generate multiple levels: $\pm V_{DC}$, $\pm 2V_{DC}$ and $\pm 3V_{DC}$ and 0 without the need for multiple DC sources or conventional boost transformers, in which V_{DC} is the input DC voltage, V_{out} is the output AC voltage, V_{an} is the voltage at point a, V_{bn} is the voltage at point b, and V_{ab} is the output voltage between points a and b. In addition, the relationship between the modulation index and the input voltage $V_{in} = V_{DC}$ and the output voltage V_{out} is expressed by the following formula:

$$V_{out} = V_{ab} = V_{an} + V_{bn} = V_{an} - V_{bn} \quad (2)$$

$$V_{out} = M_a.3E \quad (3)$$

With $M_a = 1$ as the modulation index, representing the ratio between the amplitude of the reference signal and the DC voltage amplitude, $E = V_{DC} = V_{in}$ is the input voltage, and the factor 3 reflects the maximum voltage boosting capability with $V_{out} = V_{ab,max} = 3V_{DC}$. This structure operates with eight switching states summarized in Table 1 and Fig. 1 as follows:

Table 1. Switching states and key voltages of the proposed 8S7L-BSCI topology

States	S_1 ($\bar{S}_2$)	S_3 ($\bar{S}_4$)	S_5 ($\bar{S}_6$)	S_8 ($\bar{S}_7$)	V_{out}	V_{C1}	V_{C2}	V_{CD}
I	0	0	1	1	0	↑	↑	–
II	1	0	1	1	V_{DC}	↓	–	↑
III	0	1	1	1	$2V_{DC}$	↑	↑	–
IV	1	1	1	1	$3V_{DC}$	↓	–	↑
V	0	0	0	0	0	↑	↑	–
VI	1	0	0	0	$-V_{DC}$	↓	–	↑
VII	0	1	0	0	$-2V_{DC}$	↑	↑	–
VIII	1	1	0	0	$-3V_{DC}$	↓	–	↑

0 - Switch OFF; 1 - Switch ON; – No change; ↑ Increases, ↓ Decreases;

The modulation index M_a indicates how much percentage of the maximum output voltage is achieved. When $M_a = 1$, the maximum output voltage is $3V_{DC}$. If M_a decreases (0.7, 0.4, 0.2…), the output voltage decreases accordingly, the power is reduced, and the waveform becomes more distorted because the voltage steps remain unchanged. As M_a increases from 0 to 1, the output voltage gradually rises to the maximum, but it must not exceed 1 to avoid distortion and saturation.

State (I) in Fig. 1 (a), switches S_2, S_4, S_5, and S8 are ON, while S_1, S_3, S_6, and S_7 are OFF. In this state, the DC source V_{DC} charges capacitor C_1 through S_2 and diode D_1 and simultaneously charges C_2 through S_4 and D_2, thereby both capacitors reach a balanced voltage level V_{C1} and V_{C2}. The load current flows through the H-bridge branch S_5-S_8, but since points a and b are at the same voltage level, $V_{ab} = 0$. During this state, D_1 and D_2 are forward-biased, while the diodes in parallel with S_1, S_3, S_6, and S_7 are reverse-biased. Switch S_2 is controlled by high-frequency PWM to precisely regulate the charging current of C_1, whereas S_4 and S_5-S_8 are switched at low frequency to reduce losses and stabilize the state.

State (II) in Fig. 1 (b), switches S_1, S_4, S_5, and S_6 are ON, while the remaining switches are OFF. In this state, the input source V_{DC} is applied directly to the load through the path S_1-S_4-load-S_6-S_5, generating the level $V_{ab} = +V_{DC}$. Capacitor C_1 continues to be charged and maintained at the level of S_1 and D_1, while C_2 keeps its voltage via S_4. Diodes D_1 and D_2 do not conduct significant current, only providing support when rebalancing is needed. Switch S_1 continues to operate with high-

frequency PWM to modulate the output pulse width, while S_4, S_5, and S_6 are switched at the fundamental frequency to reduce losses.

State (III) in Fig. 1 (c), the output voltage is increased by turning OFF S_1 and turning ON S_2, S_3, S_5, and S_8. In this case, capacitor C_1 is connected in series with the source V_{DC} through S_2 and D_1, producing an output voltage, which is expressed as

$$\begin{cases} V_{C1} = V_{DC} \\ V_{C2} = V_{DC} + V_{C1} = 2V_{DC} \\ V_{out} = V_{ab} = V_{an} + V_{bn} = V_{DC} + V_{C1} = 2V_{DC} \end{cases} \quad (4)$$

The current flows from the positive terminal through S_2, across C_1, then continues through S_3 and the load, and returns to the negative terminal via S_5-S_8. Diode D_1 conducts to ensure that C_1 charges/discharges in the correct direction, while D_2 is reverse-biased. S_2 is controlled with high-frequency PWM to stabilize the voltage of C_1, whereas S_3, S_5, and S_8 are switched at low frequency to reduce losses.

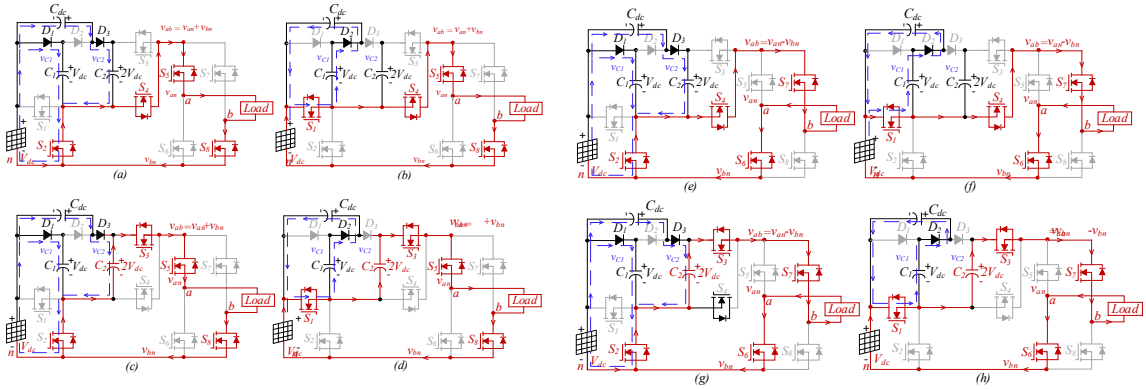


Fig. 1. The operating states of 8S7L-BSCI with (a) $V_{out} = 0$; (b) $V_{out} = +V_{DC}$; (c) $V_{out} = +2V_{DC}$; (d) $V_{out} = +3V_{DC}$; (e) $V_{out} = 0$; (f) $V_{out} = -V_{DC}$; (g) $V_{out} = -2V_{DC}$; (h) $V_{out} = -3V_{DC}$

State (IV) in Fig. 1 (d), the output voltage is further increased by turning OFF S_2 and turning ON S_1 together with S_3, S_5, and S_8. At this moment, the voltage across capacitor V_{C1} and the voltage of capacitor V_{C2} are connected in series with the source through S_1 and S_3, producing an output voltage, expressed as:

$$\begin{cases} V_{C1} = V_{DC} \\ V_{C2} = V_{DC} + V_{C1} = 2V_{DC} \\ V_{out} = V_{ab} = V_{an} + V_{bn} = V_{C1} + V_{C2} = 3V_{DC} \end{cases} \quad (5)$$

The current flows from the positive terminal through S_1, sequentially across C_1 and C_2, then continues through S_3 and the load, and finally returns to the negative terminal via S_5-S_8. Both diodes D_1 and D_2 are reverse-biased to block undesired discharging paths. S_1 is controlled with high-frequency PWM to precisely regulate the duration of the $+3V_{DC}$ level, while S_3, S_5, and S_8 are switched at low frequency to minimize losses.

State (V) in Fig. 1 (e) The system returns to the neutral level of 0 V, by turning ON S_2, S_4, S_6, and S_7. At this point, node a is connected to the positive terminal through S_1-S_3, while node b is connected to the positive terminal through S_6-S_7, resulting in $V_{ab} = 0$. Capacitors C_1 and C_2 maintain their voltages from the previous state due to the stored energy. Diodes D_1 and D_2 remain reverse-biased. Switch S_2 continues to operate with high-frequency PWM to ensure voltage balancing of C_1, while S_4, S_6, and S_7 are switched at low frequency.

State (VI) in Fig. 1 (f) The circuit begins the negative half-cycle by turning OFF S_2, S_3, S_5, and S_8, and turning ON S_1, S_4, S_6, and S_7. At this point, the H-bridge reverses the polarity, and the source V_{DC} is applied to the load in the opposite direction, producing $V_{ab} = -V_{DC}$. The current flows from

point b through S_7-S_6, then through the load to point a, and returns to the source through S_3-S_2. Capacitor C_1 maintains its voltage via S_1 and D_2. S_1 is controlled with high-frequency PWM to regulate the $-V_{DC}$, level, while the other switches operate at low frequency to reduce losses.

State (VII) in Fig. 1 (g) In this state, S_2, S_3, S_6, and S_7 are ON, and capacitor C_1 is connected in series with the source V_{DC}, but with reversed polarity. The total voltage is

$$\begin{cases} V_{C1} = V_{DC} \\ V_{out} = V_{ab} = V_{an} - V_{bn} = -(V_{DC} + V_{C1}) = -2V_{DC} \end{cases} \quad (6)$$

The load current flows from point b through S_7 and S_6, then through the load to point a, and returns via S_3-S_2. Diode D_2 does not conduct, while D_1 is reverse-biased to prevent undesired discharge. Switch S_2 operates at high-frequency PWM to control the duration of the $-2V_{DC}$ level, while S_3, S_6, and S_7 are switched at low frequency, ensuring a stable transition from $-V_{DC}$ to $-2V_{DC}$.

State (VIII) in Fig. 1 (h), the circuit further increases the negative voltage level by turning OFF S_2 and turning ON S_1 along with S_3, S_6, and S_7. At this moment, the source V_{DC}, capacitor C_1, and capacitor C_2 are connected in series but with reversed polarity, producing

$$\begin{cases} V_{C1} = V_{DC} \\ V_{C2} = V_{DC} + V_{C1} = 2V_{DC} \\ V_{out} = V_{ab} = V_{an} - V_{bn} = -(V_{C1} + V_{C2}) = -3V_{DC} \end{cases} \quad (7)$$

The current flows from point b through S_7-S_6, through the load to point a, and then returns to the source via S_3, C_1, C_2, and S_1. Diodes D_2 is reverse biased to block reverse current into the source. Switch S_1 is controlled with high-frequency PWM to regulate the duration of the $-3V_{DC}$ level, while S_3, S_6, and S_7 are switched at low frequency to reduce losses and ensure a smooth transition from $-2V_{DC}$ to $-3V_{DC}$.

2.2. Carrier-Based Pulse-Width Modulation of the Proposed 8S7L-BSCI Configuration

The PWM modulation method of the proposed 8S7L-BSCI topology employs three triangular carriers T_1, T_2 and T_3 with the same phase, frequency f_s, and amplitude E. These carriers are vertically arranged along the voltage axis as follows: T_1 oscillates within the range 0 to E; T_2 oscillates within the range E to $2E$; and T_3 oscillates within the range $2E$ to $3E$. They are compared with the rectified sinusoidal reference signal V_{ref} to generate independent preliminary gating signals for switches S_1 through S_4, as illustrated in Fig. 2 (a).

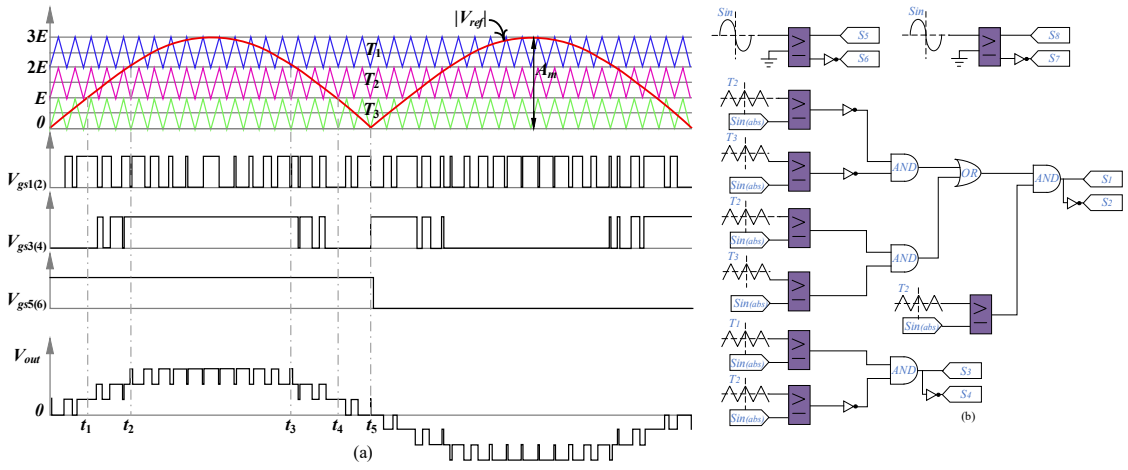


Fig. 2. Typical PWM modulation waveforms (a) and (b) Logic for generating switch gating signals

With this arrangement, the inverter synthesizes all seven voltage levels, with the modulation index calculated accordingly:

$$M_a = \frac{A_m}{3E} \tag{8}$$

In which A_m is the peak amplitude of the sinusoidal reference wave. By using logic gates to select the state occurring after comparing the reference wave and the carrier waves, as described in Fig. 2 (b), the triggering instants of the switch pair S_5 and S_8 in Fig. 2 (a) are determined according to the state table. To ensure low overall switching losses, the control scheme is designed such that switches S_3, S_4, S_5 (S_8), and S_6 (S_7) operate at low frequency, while the other switches, namely S_1 and S_2, operate at high frequency (PWM). However, the voltages across them are usually clamped at low levels by capacitors C_1 and C_2. Therefore, the use of the multi-carrier PWM method produces seven output voltage levels that approximate a sinusoidal waveform while ensuring capacitor voltage balance.

3. Comparison of the Proposed 8S7L-BSCI Topology with Existing Multilevel Inverters

The seven-level single-phase boost inverter structure based on the switched-capacitor configuration with eight switching devices employs a total of eight switches, with eight main switches S_1-S_4 and a full H-bridge configuration S_5-S_8 functioning to generate both positive and negative voltages. When compared with existing multilevel inverter structures such as NPC [2], Flying Capacitor (FC) [1], CHB (Cascaded H-Bridge) [21] and other boost-type switched-capacitor inverters, the proposed configuration demonstrates several advantages, achieving significant hardware efficiency with a low switch-per-level ratio of about 1.14 – still lower than others. It also offers the benefit of not requiring multiple DC sources or complex voltage-balancing circuits while maintaining inherent boosting capability similar to recent SC-MLI structures [32], [34]. Specifically, this structure uses only a single DC source but is capable of generating seven output voltage levels $N_{VL} = 7$ with only 8 switches $N_s = 8$ resulting in a switch-per-level ratio as follows:

$$SPRL = \frac{N_S}{N_{VL}} \tag{9}$$

The $SPRL$ is about 1.14, in which N_s is the number of switching devices and; N_{VL} is the number of voltage levels. In addition, the configuration also integrates two floating capacitors C_1, C_2 and three diodes D_1-D_3 to perform the charging and discharging functions cyclically, enabling the generation of higher voltage levels without requiring a discrete boost converter. The self-voltage balancing capability of the capacitors is ensured through a sequential control strategy, without the need for complex control circuits as in [1], [2]. The Total Standing Voltage $TSV = 7$ in the 8S7L-BSCI structure includes the two capacitors C_1, C_2 and the three clamping diodes (V_{dj}; $j = 1$ to 3). The maximum reverse voltage V_s of each switch is referenced to the DC voltage V_{DC}; using eight switches, the device blocking voltages of switches S_1 to S_8 (V_{si} with $i = 1$ to 8) are determined in equation (1). The total standing voltage (TSV) [32] of all semiconductor devices, after normalization with respect to the maximum output voltage $V_{out\text{-}max}$ is expressed in per unit (pu) as follows:

$$TSV = \left(\sum_{i=1}^{8} V_{Si} + \sum_{j=1}^{3} V_{dj}\right) / (n_{vb} V_{DC}) \tag{10}$$

With $n_{vb}=V_{out\text{-}max}/V_{DC}$ as the boost ratio between the maximum output voltage $V_{out\text{-}max}$ and the input voltage V_{DC}, which is controlled through the sequential arrangement of the switched-capacitor stages and the uniform voltage distribution across the switches, the proposed topology achieves values higher than some structures but significantly lower than others, as summarized in Table 2. for seven-level inverters of type V_{gs1}. At the same time, this index remains greater than the TSV of five-level and nine-level inverters. The normalized voltage factor n_{vb} is greater than 1, making this configuration particularly suitable for low-voltage PV systems. Meanwhile, these MLIs employ more

switches, thus requiring additional gate driver circuits. The comprehensive Cost Function (*CF*) [41] is expressed by the following formula:

$$CF = N_{Dr} + N_S + N_D + N_C + \alpha.\frac{TVS}{n_{vb}} \quad (11)$$

where $N_{Dr} = N_s$ is the number of driver circuits, N_c is the number of capacitors, N_d is the number of diodes, and α is the loss factor depending on the semiconductor material Si, SiC,.., taken as 1 or 2.

The proposed 8S7L-BSCI topology structure exhibits a much lower *CF* compared to other SCMLI configurations that use 10 to 12 switches to achieve the same output voltage level as in [13], [40]. Although the *CF* does not account for capacitor capacity, actual operating voltage, and capacitor ripple when calculating the monetary cost, the 8S7L-BSCI configuration remains highly competitive thanks to the reduced number of components, *TSV*, and $n_{vb} \approx 3$, which are optimal. In MLI structures with $n_{vb} \geq 1$, the 8S7L-BSCI configuration with a boost factor of 3 outperforms MLIs V_{gs1} [25], [55] and $n_{vb} \leq 1$ [32], as well as five-level MLIs with a boost factor of 2. Although it employs more switches than in [32], the full H-bridge structure allows flexible modulation capability and reduces the requirements for polarity reversal techniques. At the same time, the voltage balancing capability of the flying capacitors C_1 and C_2 is ensured through the symmetrical charging/discharging process across the switching states in Table 2. Table 2. Thereby avoiding the imbalance phenomenon commonly found in SC-MLIs without balancing control [41]. With multilevel output characteristics and integrated boosting capability, this configuration reduces filtering requirements, improves efficiency, and decreases electromagnetic losses. The 8S7L-BSCI configuration achieves a good compromise between moderate hardware complexity, integrated boosting, flexible polarity reversal, reasonable component count, and high waveform quality, making it a promising, efficient, and economical MLI solution for low- to medium-power applications.

Table 2. Comparison of the proposed topology with existing single-source MLIs

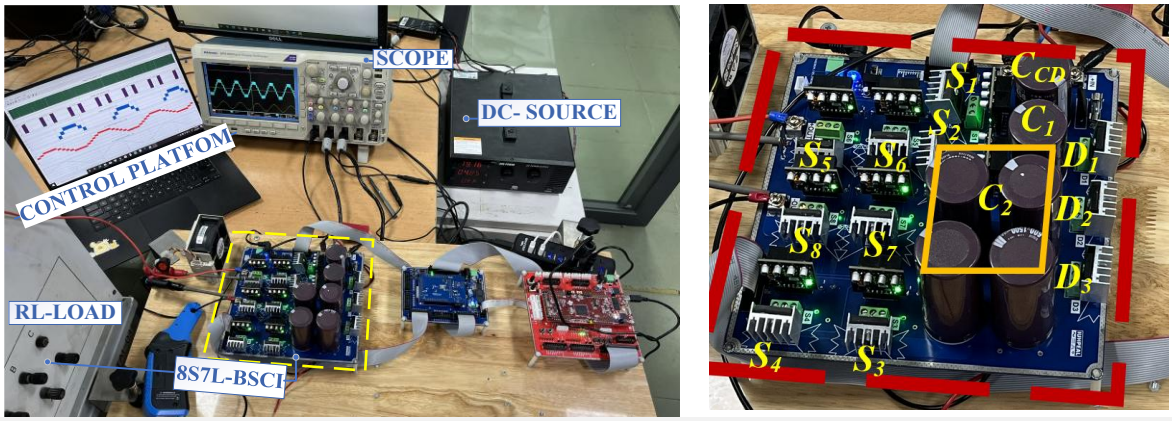
MLIs	N_{VL}	N_S	N_D	N_C	n_{vb}	*TVS (pu)*	*CF (α=1)*	*CF (α=2)*
[4]	9	12	0	2	2	5.25	21.00	29.00
[11]	7	8	4	2	1.5	4.00	25.00	29.00
[13]	7	10	0	2	1.5	7.33	26.89	31.77
[28]	5	9	0	1	2	4.5	21.25	23.25
[32]	7	6	4	3	3	6.00	21.00	23.00
[34]	5	7	2	3	1	6.00	25.00	32.00
[40]	7	11	0	2	2	5.5	21.00	29.00
[55]	7	8	3	2	4	5.75	25.00	29.00
8S7L-BSCI	7	8	3	2	3	7	23.33	25.66

4. Simulation and Experimental Results of the Proposed 8S7L-BSCI Configuration

The 8S7L-BSCI inverter configuration consists of two cascaded switched-capacitor stages and a full H-bridge, enabling the generation of seven output voltage levels. A 350W 8S7L-BSCI inverter prototype was developed to comprehensively validate the predicted characteristics from the analytical model. The system uses a 50 V_{DC} source further filtered by a parallel capacitor to suppress high-frequency current ripple. Two low-R_{ds}(on) N-channel MOSFETs switching at 25 kHz perform the seven-level modulation stage, while six 600 *V* MOSFET operating only at the grid frequency of 50 Hz serve for polarity reversal Table 3. and Fig. 3. By separating high-and low-frequency operations, the driver circuit reduces half of the PWM gate count compared with conventional SC-MLI structures, thereby lowering control cost, switching losses, and EMI radiation. In steady-state operation, the measured output voltage is 106 V_{RMS}, exhibiting seven nearly symmetrical levels; the three intermediate steps of 50 *V*, 100 *V*, and 150 *V* appear correctly across the two floating capacitors C_1 and C_2, enabling a peak voltage of ± 150 *V* corresponding to a voltage boosting factor of $n \approx 3$.

This demonstrates that Fig. 4 shows that as the modulation index M_a increases from 0.2 to 1, the output voltage V_{out} amplitude gradually rises, while the waveform becomes smoother and more

sinusoidal. At $M_a = 0.2$, the output contains only a few voltage steps with low amplitude; at $M_a = 1$, the waveform reaches the full seven-level range with maximum amplitude $V_{ab,max} = 3\ V_{DC}$. The DC-link voltage V_{DC} remains constant, confirming stable capacitor voltage balancing. The output current I_{out} becomes more sinusoidal and its amplitude increases proportionally to V_{out}.



(a) (b)

Fig. 3. (a) Experimental setup of the prototype; (b) Detailed experimental setup of the 8S7L-BSCI configuration

Table 3. Components of the 8S7L-BSCI prototype

Parameters	Values	Quantity
Input voltage (V_{DC})	50 V	1
Capacitors link (C_{CD})	450 µF	1
Capacitors link (C_1)	450 µF	1
Capacitors link (C_2)	4x1500 µF (parallel)	1
Diode (D_1, D_2 and D_3)	RHRG75120	3
MOSFET	60N100	8
R load	32 Ω	1
R load with LC filter	32 Ω, 1mH, 1µF	1
RL load	79mH + 32 Ω	1

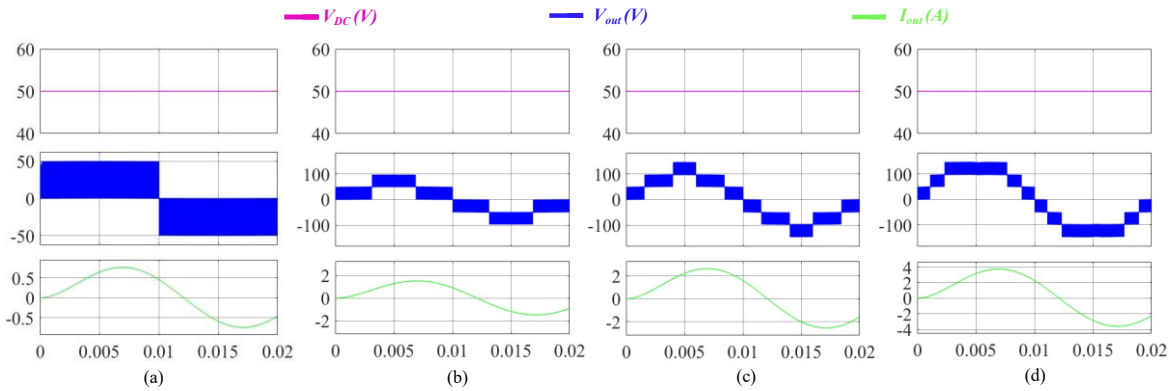


Fig. 4. Simulation Results with M_a; (a) $M_a = 0.2$; (b) $M_a = 0.4$; (c) $M_a = 0.7$; (d) $M_a = 1$

The simulation and experimental results were evaluated under three load conditions Fig. 5 and Fig. 6, including resistive load (R), inductive load (RL), and resistive load with LC filter (R–LC), in order to evaluate the influence of each load type on output voltage quality, current waveform, power factor, and harmonic filtering capability. With resistive load R Fig. 5 (a)-(b), Fig. 6 (a), the output voltage signal appears as an unfiltered stepped waveform, transmitted directly to the load, leading to a significant level of harmonic distortion Fig. 6 (c) current I_{out} -THD_R = 21.54%. Current and voltage are in phase; the current waveform still retains a stepped shape because the resistive load has no filtering ability. When adding an inductor (RL load) in Fig. 5 (c)-(d), Fig. 6 (d), the inductor acts as

a high-order harmonic filter, smoothing the current compared with the R load. The current I_{out}-THD_{RL} is reduced to 0.18%. The output current waveform approaches a sinusoidal shape, while the output voltage remains stepped. This configuration offers high filtering effectiveness, but at the expense of reduced real power transfer efficiency due to reactive power. With resistive load combined with LC filter (R–LC), as show in Fig. 5 (e)-(f), Fig. 6 (e), the current waveform becomes the smoothest and closest to sinusoidal among all three cases. Although the current I_{out} -$THD_{R(LC)}$ increases slightly to 0.52%. The voltage waveform remains stepped; however, the current is significantly filtered, effectively reducing stress on the load and semiconductor devices. This configuration exhibits the best power quality but requires stricter control and stability due to the risk of LC resonance. The load type should be selected according to application requirements: the R load provides good power efficiency but poor waveform quality; the RL load reduces harmonic distortion; and the R–LC load achieves an optimal balance between waveform quality and harmonic filtering, making it suitable for applications demanding high power quality. The capacitors demonstrate stable self-balancing behavior. In Fig. 5 (g), the blocking voltages are reasonably distributed with V_{ds},S_5 and $V_{ds,S6}$ ~150 V; in Fig. 5 (h), $V_{ds,S1}$ ~50 V and $V_{ds,S3}$ ~100 V; and capacitor voltages V_{C1}, V_{C2} quickly reach and maintain 50 V and 100 V, respectively. The experimental results in Fig. 6 (a) and Fig. 6 (b) confirm this trend: switch voltages and capacitor voltages closely match the simulations, with only minor oscillations due to device characteristics, which do not affect the system's voltage balancing and stability.

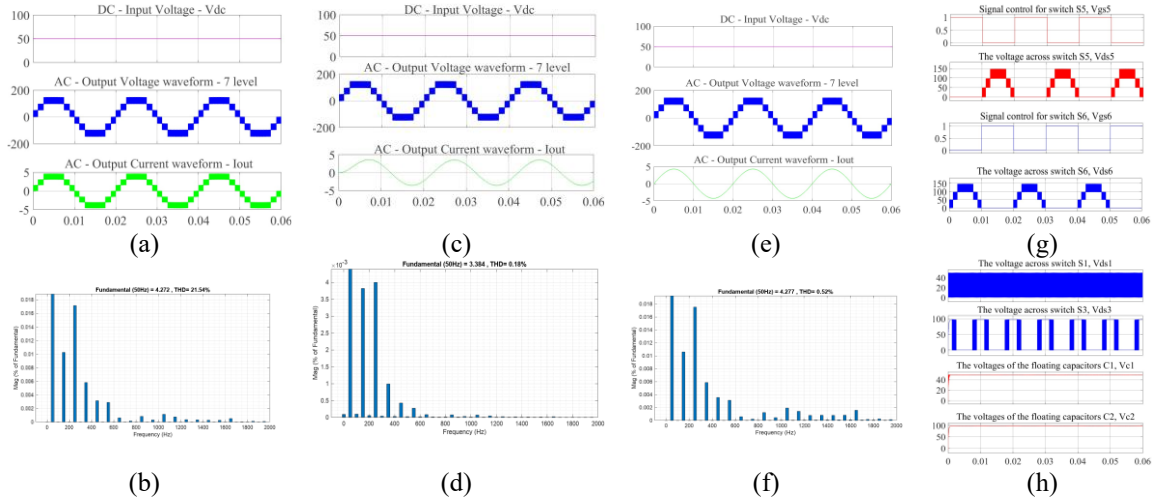


Fig. 5. Simulation results of the proposed 8S7L-BSCI configuration (a)-(b) R load, (c)-(d) RL load, (e)-(f) R load with LC filter from top (a) V_{DC} = 50V, V_{out} = 150V, and I_{out} = 5A; (b) I_{out} - THD_R = 21,54% (c) V_{DC} = 50V, V_{out} = 150V, and I_{out} = 3.5A; (d) I_{out} - THD_{RL} = 0,18%; (e) V_{DC} = 50V, V_{out} = V_{out} -(LC) = 150V and I_{out} = 4.3A; (f) I_{out} - $THD_{R\text{-}LC}$ =0,52%; (g) $V_{gs,S5}$, $V_{ds,\ S5}$, $V_{gs,S6}$, and $V_{ds,S6}$ = 150V; (h) $V_{ds,S1}$ = 50V; $V_{ds,S3}$ = V_{C2} =100V and V_{C1} = 50V

Efficiency and thermal performance of the 8S7L-BSCI configuration in Fig. 7. Experimental results show that the inverter operates stably within the 50 to 350W range, with the efficiency maintained at 95% ± 1.3% as depicted in Fig. 7 (a). The MOSFET temperature in Fig. 7 (b) rises from 28°C to approximately 75°C yet remains within the safe operating limits, owing to the fact that only two switches operate at high frequency. The maximum measured efficiency reaches 96.1% at 330 W and 73°C under a DC input voltage of 50 V and an AC output voltage of 106 V_{RMS}.

Compared with other structures in Table 4. the efficiency of the 8S7L-BSCI is slightly lower than that of some highly optimized configurations achieving 97-98%, but it still falls within the high-performance range among single-DC-source MLIs. Its thermal behavior is reliable. Given its reduced component count, inherent capacitor self-balancing, and high voltage boosting capability, the proposed topology is well suited for low-to medium-power applications such as single-phase PV inverters and energy-storage interface converters. Both simulation and experimental results demonstrate low THD_i in Fig. 7 (c), with the RL experimental load achieving the lowest distortion of 0.8%, whereas the pure resistive load produces higher THD_i. Deviations from the simulation in

Fig. 5 are primarily caused by ESR/ESL effects, parasitic inductance, and dead time, but the overall trend remains consistent: the RL load always yields the lowest THD_i. Under sudden load changes, the capacitor voltages may experience slight deviation, but the system quickly re-stabilizes within a few PWM cycles.

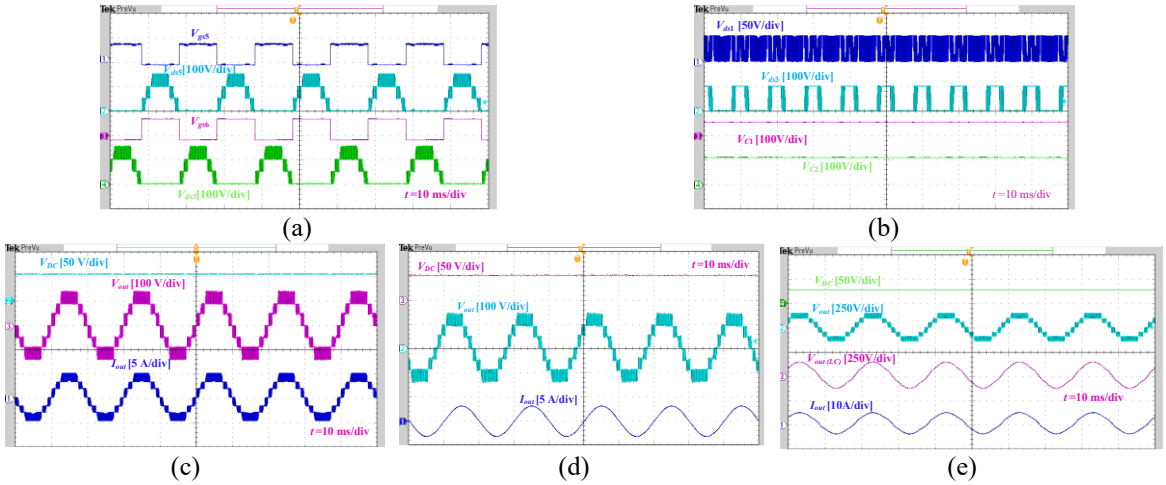


Fig. 6. Experimental results of the proposed 8S7L-BSCI configuration when operating with resistive load, inductive load, or resistive load with LC filter (c)-(e) from top. (a) $V_{gs,S5}$, $V_{ds,S5}$ (150V/div), $V_{gs,S6}$, $V_{ds,S6}$ (150V/div); (b) $V_{ds,S1}$ (50V/div), $V_{ds,S3}$ (100V/div), V_{C1} (50V/div), V_{C2} (100V/div); (c) With resistive load R - V_{DC} (50V/div), V_{out} (150V/div) and I_{out} (5A/div); (d) RL load - V_{DC} (50V/div), V_{out} (150V/div), and I_{out} (3.5A/div); (e) Resistive load R and LC filter - V_{DC} (50V/div), V_{out} (150V/div), $V_{out\text{-}(LC)}$ with LC filter (150V/div) and I_{out} (4.3A/div)

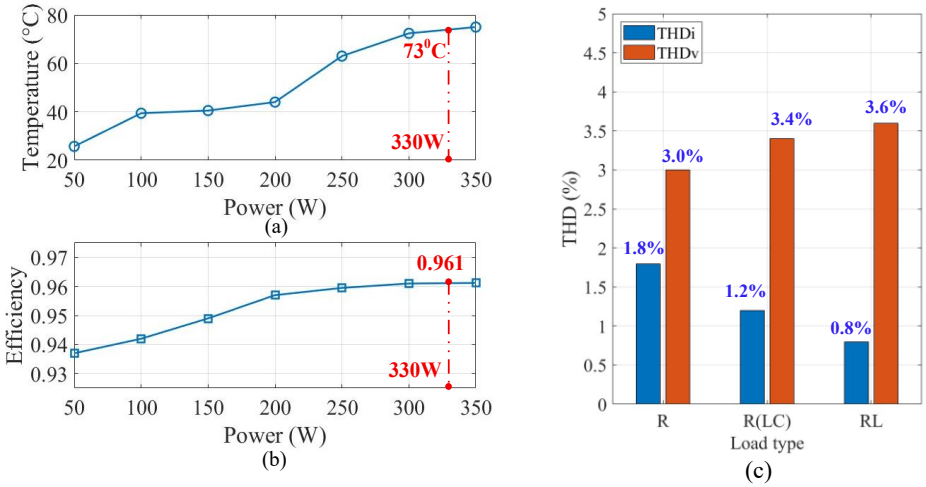


Fig. 7. Results of efficiency, thermal performance, and THD (a) Measured efficiency and (b) measured thermal characteristics with a DC input voltage of 50 V and an AC output voltage of 106 V_{RMS} (c) THD of the proposed 8S7L-BSCI configuration when operating with a resistive load R=32 Ω, an inductive load RL = 32 Ω +79 mH, and a resistive load combined with an LC filter 32 Ω, 1 mH, 1 µF

Finally, consistent with theoretical predictions based on the Cauer loss model: low conduction losses due to small and reduced clamping voltage; significant reduction in switching losses since only two switches are PWM-operated; losses on floating capacitors and diodes are limited by short charge-discharge cycles. These results place the 8S7L-BSCI on par with, or even superior to, contemporary seven-level SC-MLI structures in terms of switch-per-level ratio, triple boosting capability with two boosting stages, simple gate control scheme, reduced driver cost, and overall efficiency while highlighting its potential applications in single-phase PV inverters, energy storage systems, and residential microgrids requiring compact size, high efficiency, and cost-effectiveness.

Table 4. Experimental comparison of the proposed topology with existing single-DC-source MLIs

MLIs	N_{VL}	N_S	N_D	N_C	n_{vb}	TVS (pu)	η	t (°C)
[4]	9	12	0	2	2	5.25	92.9%	N/A
[11]	7	8	4	2	1.5	4.00	98.2%	N/A
[13]	7	10	0	2	1.5	7.33	98.3%	70 °C
[28]	5	9	0	1	2	4.5	97.91%	N/A
[32]	7	6	4	3	3	6.00	97% ± 1.3%	N/A
[34]	5	7	2	3	1	6.00	95.95%	N/A
[40]	7	11	0	2	2	5.5	93%	N/A
[55]	7	8	3	2	4	5.75	96.4%	N/A
8S7L-BSCI	7	8	3	2	3	7	95% ± 1.3%	73 °C

5. Conclusion

The 8S7L-BSCI inverter proposed in this study is an efficient solution with a simple hardware structure, using only eight switching devices to generate a seven-level output voltage with a threefold boosting capability. This is achieved by combining multistage switched-capacitor cells with a full H-bridge for polarity reversal. By using only two high-frequency PWM switches and six low-frequency switches, the design reduces switching losses due to the reduced number of high-frequency switches, simplifies the control circuit, and lowers gate-driver costs. Both simulation and experimental results have verified the self-voltage-balancing capability of the floating capacitors, the high quality of the output voltage, and the high operating efficiency. Compared with other SC-MLI configurations in the same category, the 8S7L-BSCI achieves equivalent or even superior performance with fewer components, making it highly suitable for single-phase PV applications, energy storage systems, and microgrids that demand compact size and high efficiency. Alongside the achieved advantages, the topology still presents several promising directions for further development. In future work, the configuration can be scaled to higher power levels and extended to a three-phase version. These directions will further enhance the applicability and reliability of the 8S7L-BSCI in practical power-electronics systems.

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