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Leakage Current Reduction Technique for Four-Level Capacitor Clamped Inverters

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ABSTRACT

Transformerless inverters (TIs) are widely applied in grid connected photovoltaic (PV) systems due to their advantages of high efficiency and low cost. However, the absence of galvanic isolation can result in ground leakage currents caused by the parasitic parameters of the PV system, leading to safety concerns and degraded power quality. This paper focuses on reducing the leakage current of the existing single phase BIH6 inverter by introducing an improved PWM modulation strategy. In the BIH6 structure under conventional control, the common-mode voltage (CMV) still oscillates around $V_{dc}/2$, causing the leakage current to potentially exceed 100 mA. In this study, a new modulation technique is applied to the BIH6 inverter to eliminate the zero-switching state among its eight operating states. Removing this state enables the CMV to remain constant throughout the entire switching process, thereby contributing to the reduction of leakage current. Although the number of output voltage levels decreases due to the removal of one switching state, the total harmonic distortion (THD) of both output voltage and current remains below 5%, and the inverter efficiency reaches 95%, meeting power quality requirements for grid connected PV systems. The paper provides a detailed explanation of the operating principles, mathematical modeling, and the proposed control methodology for the inverter, along with the implementation of a grid current synchronization strategy. Simulation results are included to validate the feasibility of the proposed control method. In addition, a hardware prototype has been developed using the TMS320F28379D digital signal processor (Texas Instruments, Dallas, Texas, USA) in combination with an Altera Cyclone® IV EP4CE22F17C6N FPGA platform (Intel Corporation, Santa Clara, California, USA).

1. Introduction

In recent years, transformerless inverters (TIs) have been widely adopted in renewable energy systems, particularly photovoltaic (PV) grid connected installations [1]–[4], due to their high conversion efficiency, compact design, and reduced system cost [5]–[11]. However, the elimination

of galvanic isolation introduces new challenges in terms of electrical safety and power quality, especially the issue of leakage current arising from common-mode voltage (CMV) fluctuations.

In grid connected PV systems, the inverter needs a high and stable DC-link voltage to work properly with the grid. One common way to reach this voltage is by connecting many PV panels in series. However, this setup can cause uneven performance between panels, especially if some are weaker or shaded, which affects the output of the entire system [12]–[20]. It also leads to a bulky and space consuming installation. Another way to increase the DC-link voltage is by using DC-DC converters such as buck, boost, buck-boost, and others. However, these converters cause power loss and increase system cost. To address the voltage boosting issue in traditional inverter systems, several studies have proposed using shoot through states to raise the DC-link voltage [21]–[38]. This method improves the inverter's operating capability without the need for an additional boost stage, however, using multiple inductors and capacitors increases the size, weight, and cost of the power system.

Beyond voltage boosting, transformerless operation also introduces safety and electromagnetic interference issues due to CMV fluctuations. Therefore, modern inverter research has focused on integrating voltage boosting and CMV suppression within a single structure to simultaneously improve both efficiency and safety. According to the VDE 0126-01-01 standard, the RMS leakage current must remain below 300 mA [39]–[40]. Leakage current depends on several factors, such as the output filter, the impedance of the power grid, and the parasitic capacitance (C_{PV}) between the PV system and the ground. The value of C_{PV} typically falls within the nF range and is influenced by factors such as the frame of the PV module, the type of photovoltaic cell, weather conditions, and the EMC filter.

To deal with the leakage current issue, many methods have been studied, including the development of model predictive control (MPC) algorithms. This approach is used to estimate the system's future behavior and improve the control signals. It works by using a cost function that is built based on predefined control goals and follows certain optimization rules to increase system performance [41]–[45].

In addition, using output filters such as LC or LCL helps reduce noise and harmonics, improve signal quality, and increase the system's stability and overall efficiency [46]–[51]. At the same time, an optimized modulation strategy is applied to remove unwanted switching states in the circuit, which effectively reduces leakage current. This method is especially useful for multilevel inverters, helping improve signal quality and enhance operating performance [52]–[58]. Among the inverter topologies of interest, common-ground multilevel inverters have gained much attention due to their ability to reduce leakage current in the system. These methods often rely on modifying the circuit structure to generate multiple output voltage levels. Thanks to the shared ground connection between the input and output, leakage current does not form in the circuit. In addition, a higher number of voltage levels helps reduce the size of the output filter. However, these inverters still have some drawbacks, such as more complex control circuits, a higher number of components, which increases cost, and difficulties in precise control, making them less suitable for high power systems [59]–[61]. These control challenges become more significant as the power level increases. The presence of multiple neutral points and auxiliary voltage branches can cause midpoint voltage imbalance and uneven voltage distribution across semiconductor devices. As the number of voltage levels increases, more sophisticated modulation and voltage balancing algorithms are required, along with high precision sensors to maintain stable capacitor voltages. Furthermore, because all negative terminals are grounded, circulating currents may appear between inverter legs, increasing losses and reducing efficiency. These limitations hinder the scalability of common ground topologies for high power systems.

Consequently, non-common-ground multilevel inverters have also been widely studied due to their flexible structure and ease of control. These inverters often use special modulation techniques and switching arrangements to generate the desired output waveform. However, controlling leakage current during switching states remains a key issue that requires further investigation [62]–[65].

Recently, an approach based on a switched capacitor network has been proposed, in which the midpoint of two capacitors is utilized during the switching process [66]–[67]. By using this midpoint, intermediate voltage levels can be generated, which helps limit the amplitude of common-mode voltage (CMV) fluctuations relative to the DC-link voltage.

In this context, the Boost-type Improved H6 (BIH6) inverter emerges as a promising candidate that simultaneously addresses both requirements. As an evolution of the H6 family, BIH6 inherently provides voltage boosting without additional DC–DC stages and enables active control of CMV through flexible switching states [68].

Although various modulation and control methods have been proposed for transformerless inverters, most existing approaches focus on either CMV reduction or voltage boosting individually, without unifying both in a simple control framework. Moreover, conventional PWM strategies for BIH6 still exhibit CMV fluctuations up to V_{dc}, leading to measurable leakage currents.

This paper aims to fill this research gap by proposing a Level-Three Pulse Width Modulation (LT-PWM) technique for the BIH6 inverter that maintains a constant CMV at $V_{dc}/2$ throughout the entire modulation cycle. The research hypothesis is that by eliminating zero switching states, leakage current can be almost completely suppressed without compromising harmonic performance.

To verify this hypothesis, the inverter performance is quantitatively evaluated based on three criteria: (i) CMV stability, (ii) RMS leakage current magnitude, and (iii) total harmonic distortion (THD) of the output voltage and current. Both simulation and experimental results show that the proposed LT-PWM method nearly eliminates the leakage current, while maintaining THD within acceptable limits, confirming its superior improvement over conventional modulation techniques.

The structure of the paper is organized as follows. Section 2 describes the operating states and common-mode voltage characteristics of the BIH6 inverter. Section 3 presents the proposed LT-PWM modulation technique and the single-phase grid synchronization control strategy. Section 4 provides both simulation and experimental results that validate the effectiveness of the proposed method under various operating conditions. Finally, Section 5 concludes the paper.

2. Operating States and Common-Mode Voltage of BIH6 Inverter

The eight operating states of the BIH6 inverter (Fig. 1) can be categorized into two main groups: active states and zero states. Active states (A, B, E, F): These are the states in which the BIH6 actively controls the output based on input conditions. These states play a crucial role in system operation, determining how energy is transferred from the PV system to the grid. Zero states (C, D): These states occur when the BIH6 does not provide output voltage to the load. They are typically used during transitions between active states or when power transfer is not required. Each of these states has a specific switching combination. Table 1 provides the switching states, showing the switching status of each device and the corresponding charging and discharging behavior of the capacitors in each operational state.

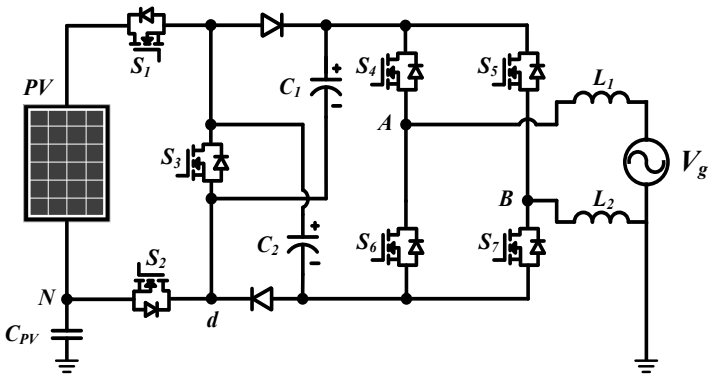


Fig. 1. The BIH6 grid-tied inverter structure

Table 1. Corresponding switching states of the BIH6 inverter

State	Switches Signals							Diode		Capacitor		Output Voltage
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	D_1	D_2	C_1	C_2	V_{AB}
A	0	0	1	1	0	0	1	Off	Off	*d*	*d*	$2V_{dc}$
B	1	1	0	1	0	0	1	*On*	*On*	*c*	*c*	V_{dc}
C	1	1	0	1	1	0	0	*On*	*On*	*c*	*c*	0
D	1	1	0	0	0	1	1	*On*	*On*	*c*	*c*	0
E	1	1	0	0	1	1	0	*On*	*On*	*c*	*c*	$-V_{dc}$
F	0	0	1	0	1	1	0	Off	Off	*d*	*d*	$-2V_{dc}$
c – Capacitor is charging; d – Capacitor is discharging												

The operating states of the semiconductor switches and the corresponding current paths are described in Fig. 2. Overall, the BIH6 inverter generates five different output voltage levels, namely 0, $\pm V_{dc}$ and $\pm 2V_{dc}$. The transitions between these switching states cause variations in the CMV across the parasitic capacitors.

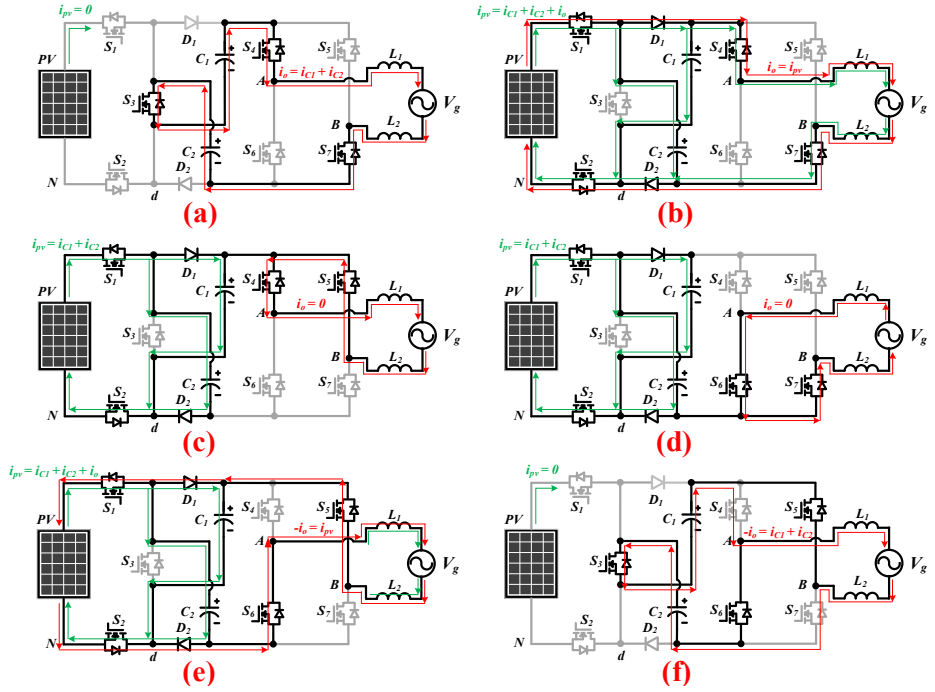


Fig. 2. The current paths for charging/discharging the capacitors in the switching states of the BIH6 inverter: (a) State A with $V_{AB} = 2V_{dc}$; (b) state B with $V_{AB} = V_{dc}$; (c) state C with $V_{AB} = 0$; (d) state D with $V_{AB} = 0$; (e) state E with $V_{AB} = -V_{dc}$; (f) state F with $V_{AB} = -2V_{dc}$

By analyzing CM noise in Fig. 1, it can be observed that the CM equivalent model can be represented in Fig. 3–(a) has four different voltage sources: v_{CPV}, v_g, v_{AN} and v_{BN}. These four sources have different frequencies; therefore, aliasing analysis needs to be considered. However, v_{CPV} and V_g mainly contain low frequency components, so they can be ignored in CM noise analysis. In contrast, v_{AN} and v_{BN} vary rapidly and are the main sources of common-mode noise.

Equation (1) is derived based on Kirchhoff's Voltage Law applied to the equivalent common-mode circuit. V_{TH} represents the open circuit voltage at the C_{PV} terminals in Fig. 3–(b):

$$v_{TH} = \frac{v_{AN}L_2 + v_{BN}L_1}{L_1 + L_2} \tag{1}$$

The voltages v_{AN} (the voltage difference between terminals A and N) and v_{BN} (the voltage difference between terminals B and N) can be expressed in terms of the CMV components. Mathematically, the CMV (v_{CM}) is defined as follows [69]:

$$v_{CM} = \frac{v_{AN} + v_{BN}}{2} \tag{2}$$

And the differential-mode voltage (DM) is defined as

$$v_{DM} = v_{AN} - v_{BN} = v_{AB} \tag{3}$$

From (2) and (3):

$$\begin{cases} v_{AN} = \dfrac{v_{DM}}{2} + v_{CM} \\ v_{BN} = -\dfrac{v_{DM}}{2} + v_{CM} \end{cases} \tag{4}$$

Equation (5) represents the Thevenin equivalent voltage observed from the terminals of the parasitic capacitor C_{pv}. It shows that the Thevenin voltage v_{TH} directly depends on the difference between the CMV and the DM. This implies that any variation in CMV during switching transitions will affect the parasitic capacitor voltage v_{CPV}, thereby generating leakage current.

Combining (1) and (4):

$$v_{TH} = v_{CM} + v_{DM}\frac{L_2 - L_1}{2(L_2 + L_1)} \tag{5}$$

According to the study presented in [70], the total common-mode noise is influenced by the DM and depends on the values of the two filter inductors L_1 and L_2. When the inductances L_1 and L_2 are selected to be equal, the DM component in (6) can be completely eliminated from the resulting CMV.

Therefore, the CMV can be expressed as follows:

$$v_{TH} = v_{CM} = \frac{v_{AN} + v_{BN}}{2} \tag{6}$$

The phenomenon of leakage current is analyzed by applying Kirchhoff's laws to the CM model, as illustrated in Fig. 3–(a).

$$\begin{cases} v_{CPV} = v_{AN} + L_1\dfrac{di_1}{dt} \\ v_{CPV} = v_{BN} + L_2\dfrac{di_2}{dt} \\ i_{CM} = i_1 + i_2 \end{cases} \tag{7}$$

From (7), the voltage across the parasitic capacitor v_{CPV} is determined by (8). Since the two inductors L_1 and L_2 have the same inductance value (assumed to be L), the equivalent inductance of the circuit will be $L/2$.

$$v_{CPV} = v_{CM} + \frac{1}{4}L\frac{di_{CM}}{dt} \tag{8}$$

According to (8), the equivalent circuit of CM noise is simplified and shown in Fig. 3–(c). In this circuit, leakage current appears when the voltage v_{CPV} across the parasitic capacitor changes over time. This variation causes a displacement current through the capacitor, leading to leakage current between the PV system and the ground. However, when L_1 and L_2 are not equal, the voltage v_{CPV} no longer depends solely on v_{CM}, but includes an additional term proportional to the differential-mode voltage v_{DM}, as shown in (9).

$$v_{CPV} = \frac{L_1 + L_2}{L_1 + L_2 + L_1L_2Cs^2}\left[v_{CM} + \frac{L_2 - L_1}{2(L_1 + L_2)}v_{DM}\right] \tag{9}$$

This cross-coupling component has a magnitude directly dependent on the inductance mismatch L_1 and L_2, causing v_{CPV} to vary with v_{DM} even when v_{CM} is maintained constant by the LT-PWM technique. Consequently, leakage current still persists because the voltage across the parasitic capacitor v_{CPV} is not perfectly constant and remains influenced by the inductor imbalance.

$$i_{CM} = -C_{PV}\frac{dv_{CPV}}{dt} \tag{10}$$

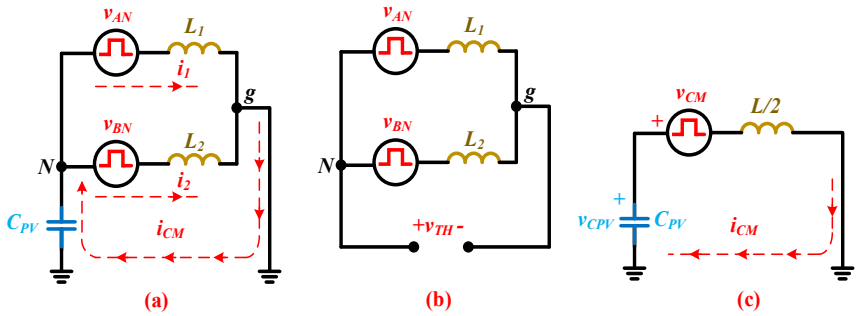


Fig. 3. Equivalent circuit diagrams: (a) Common-mode (CM) equivalent circuit; (b) Thevenin analysis; (c)Simplified common-mode (CM) equivalent circuit

From (10), it can be seen that the variation in v_{CPV} is mainly caused by the variation of the CMV, which occurs as the inverter switches between different operating states. Since v_{AN} and v_{BN} vary during these transitions, CMV is directly affected. As a result, v_{CPV}, which depends on CMV, also fluctuates. These voltage changes across the parasitic capacitor lead to the formation of leakage current in the system.

When the CMV changes, the voltage across the parasitic capacitor v_{CPV} also changes. This variation is the main cause of leakage current flowing through the capacitor C_{PV} between the PV array and the ground. Since v_{CPV} directly depends on CMV, reducing leakage current requires keeping the amplitude of CMV constant throughout the operation.

The CMV is analyzed throughout a fundamental cycle, which includes two stages: the positive half cycle and the negative half cycle. The corresponding output voltage values and CMV levels for each operating state are presented in Table 2. Based on the presented expressions, the six switching states within one cycle can cause the CMV to fluctuate with an amplitude of up to V_{dc}. Therefore, the switching states should be carefully selected and arranged so that CMV stays at a fixed amplitude during operation.

Observing the CMV values in Table 2 shows that only four switching states A, B, E, and F maintain the same CMV level of $V_{dc}/2$, whereas the two zero states (C and D) introduce large voltage steps. Therefore, restricting the modulation to the state set A, B, E and F is essential for the LT-PWM scheme to keep the CMV fixed throughout the switching cycle.

Table 2. The output voltage and common-mode voltage of the corresponding states

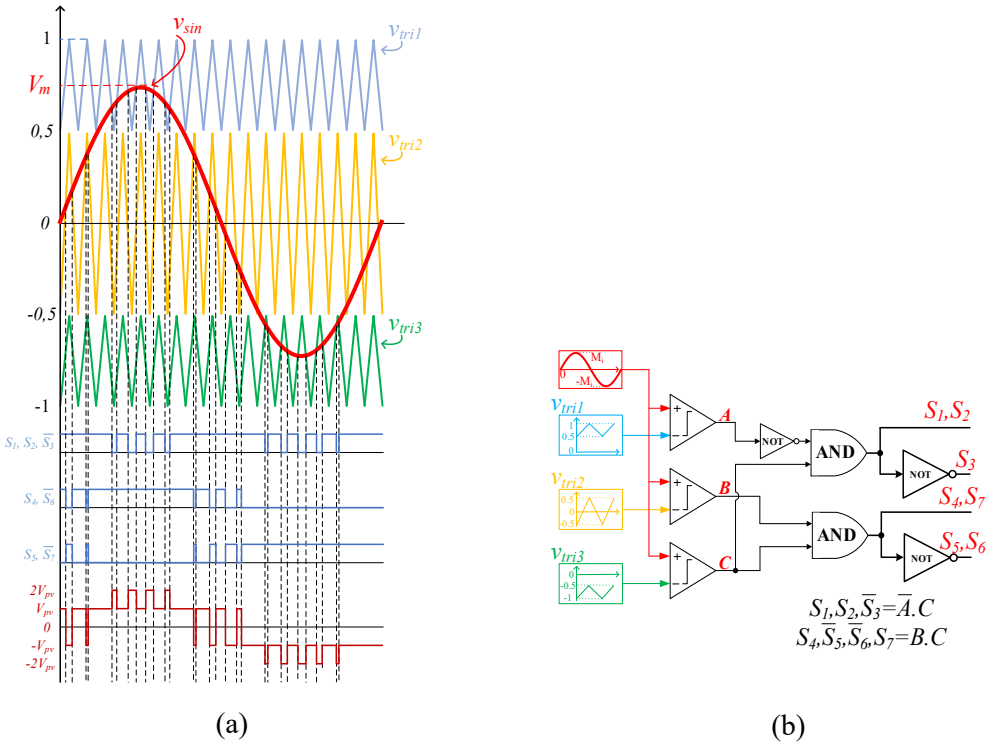
State	V_{AB}	$V_{AN} = V_{Ad} + V_{dN}$	$V_{BN} = V_{Bd} + V_{dN}$	V_{CM}
A	$2V_{dc}$	3/2 V_{dc}	$-1/2\ V_{dc}$	$V_{dc}/2$
B	V_{dc}	V_{dc}	0	$V_{dc}/2$
C	0	V_{dc}	V_{dc}	V_{dc}
D	0	0	0	0
E	$-V_{dc}$	0	V_{dc}	$V_{dc}/2$
F	$-2V_{dc}$	$-1/2\ V_{dc}$	3/2 V_{dc}	$V_{dc}/2$

3. Modulation Technique and Grid Connected Control Strategy for Four-Level BIH6 Inverter

To keep the CMV stable at $V_{dc}/2$ during the entire operating cycle, the switching states of the BIH6 inverter need to be carefully selected. Specifically, states C and D, which have CMV values of 0 and V_{dc}, cause large fluctuations in CMV and should be removed from the operating state set. Instead, only the four active states A, B, E, and F are retained, allowing V_{cm} to remain constant at $V_{dc}/2$.

To accurately control the selected switching states, the Level-Three Pulse Width Modulation (LT-PWM) technique is applied, as shown in Fig. 4–(a). Unlike the conventional level-shifted PWM method, which uses carriers with identical amplitudes, the proposed LT-PWM technique employs three level-shifted triangular carriers with different amplitude ranges v_{tri1} has an amplitude range from 0.5 to 1, v_{tri2} ranges from -0.5 to 0.5, and v_{tri3} ranges from -1 to -0.5. These carrier signals are compared with the modulation reference signal $V_{ref} = M_a sin(\omega t)$ to generate appropriate switching signals for the inverter. As a result, the method remains simple, effective, and well suited for grid connected PV systems that require high reliability.

Fig. 4–(b) depicts the logic for generating gate control signals to regulate the inverter operation. This logic employs a combination of OR gates, AND gates, and comparators to determine the switching states of the power switches. The high and low logic states of each switch, along with the control principles, are clearly defined in (11) and (12).



(a) (b)

Fig. 4. (a) LT-PWM control scheme; (b) Logic used for the gate pulse generation for BIH6

$$S_1 = S_2 = \overline{S_3} = \begin{cases} 0 & V_{tr1} \le V_{ref} \quad and \quad V_{tr3} \ge V_{ref} \\ 1 & V_{tr1} \ge V_{ref} \quad and \quad V_{tr3} \le V_{ref} \end{cases} \tag{11}$$

$$S_4 = \overline{S_5} = S_6 = \overline{S_7} = \begin{cases} 1 & V_{tr2} \le V_{ref} \\ 0 & V_{tr2} \ge V_{ref} \end{cases} \tag{12}$$

To implement grid synchronization for the BIH6 inverter using the LT-PWM method, the overall grid connected control scheme [71] is illustrated in Fig. 5. The system consists of three main functional blocks: the Phase-Locked Loop (PLL), the $dq/\alpha\beta$ transformation blocks, and the current control loop.

A PLL as shown in Fig. 6, is employed to extract the phase angle θ from the grid voltage. This phase angle is then used in the coordinate transformation process to convert voltage and current signals from the stationary $\alpha\beta$ reference frame to the synchronous dq reference frame.

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} cos\,\theta & sin\,\theta \\ -sin\,\theta & cos\,\theta \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{13}$$

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} cos\,\theta & sin\,\theta \\ -sin\,\theta & cos\,\theta \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \tag{14}$$

Equations (13) and (14) describe the standard Park transformation, which separates the active power component d and the reactive power component q. This decoupling enables the current controller to regulate the two control channels independently while maintaining phase synchronization with the grid voltage.

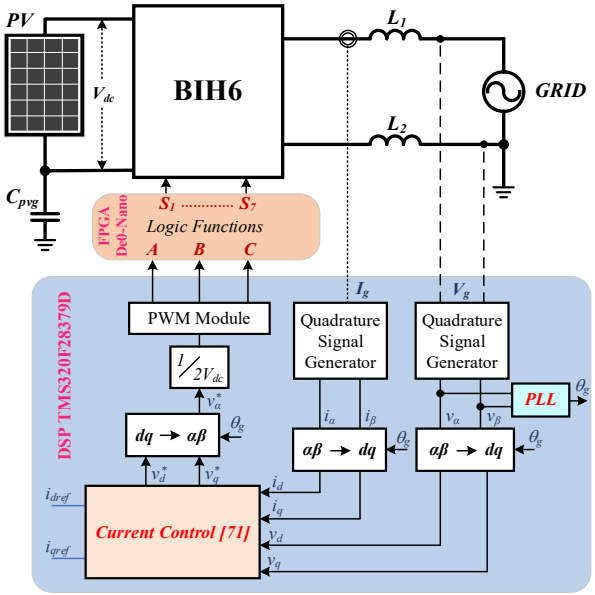


Fig. 5. Block diagram of the grid connected control system for the BIH6 inverter

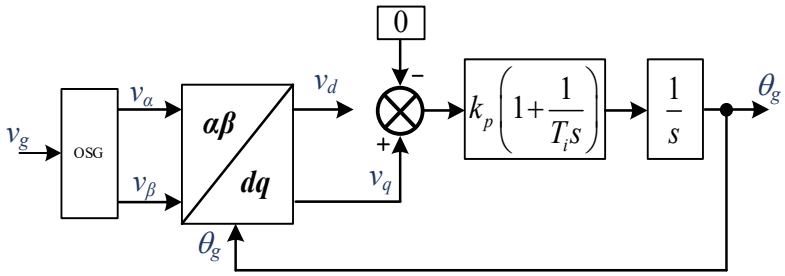


Fig. 6. Structure of the OSG-PLL

In the dq reference frame, the d axis current represents the active power component, while the q axis current corresponds to the reactive power component. Therefore, the $id - iq$ control strategy is employed to regulate the output power of the inverter, as illustrated in Fig. 7. The reference current equations are expressed as follows:

$$\begin{cases} i_{dref} = \dfrac{2.P_{ref}}{v_d} \\ i_{qref} = \dfrac{2.Q_{ref}}{v_d} \end{cases} \tag{15}$$

where P_{ref} and Q_{ref} denote the reference active and reactive powers, respectively.

Equation (15) expresses the calculation of the dq reference currents corresponding to the desired active and reactive power components, thereby enabling independent control of both power channels in the dq domain.

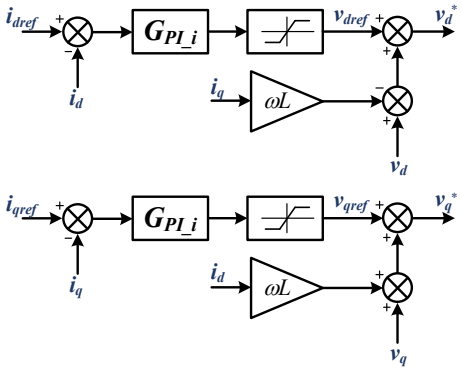


Fig. 7. Current control diagram in the dq reference frame

A PI controller is employed to minimize the error between the reference and the measured currents. Equation (16) describes the PI controller in the dq domain, which is responsible for generating the control voltages required to track the reference currents accurately and stably.

$$v_{dqref} = (i_{dqref} - i_{dq}).G_{PI\_i} \tag{16}$$

with

$$G_{PI\_i} = \frac{k_p s + k_i}{s}$$

After determining the reference voltage components in the dq reference frame, it is observed that these voltages depend on both the grid voltage and the voltage drop across the filter inductors. The expressions in (17) account for the inductor voltage drop and the cross-coupling term ωL, thereby improving the current tracking accuracy under load variations and grid voltage ripple.

$$\begin{cases} v_d^* = v_{dref} + v_d - \omega L i_q \\ v_q^* = v_{qref} + v_q + \omega L i_d \end{cases} \tag{17}$$

After obtaining the two reference voltage components v_d^* and v_q^*, (18) performs the inverse Park transformation is performed to convert them from the dq reference frame back to the $\alpha\beta$ reference frame. This process provides the reference voltage signals required for PWM pulse generation.

$$\begin{bmatrix} v_\alpha^* \\ v_\beta^* \end{bmatrix} = \begin{bmatrix} cos\,\omega\,t & -sin\,\omega\,t \\ sin\,\omega\,t & cos\,\omega\,t \end{bmatrix} \begin{bmatrix} v_d^* \\ v_q^* \end{bmatrix} \tag{18}$$

4. Simulation and Experiment Results

The switching states and voltage expressions derived in the previous analysis were validated through PSIM simulations and measurements obtained from a 500 W experimental prototype to

ensure consistency between the theoretical model and practical behavior. The proposed LT-PWM modulation technique for the BIH6 inverter was implemented and evaluated in PSIM, with the simulation parameters and circuit specifications summarized in Table 3.

To systematically analyze the operation of the BIH6 inverter, a single phase equivalent circuit is constructed under the following assumptions: the DC-link voltage is constant, all semiconductor switches are ideal, and the parasitic capacitance between the PV array and ground is modeled as $C_{pv} = 100\ nF$, based on typical values reported for PV modules [39]–[40]. The purpose of this analysis is to identify the switching state set and to derive the corresponding output voltage and CMV, thereby establishing the mechanism that leads to leakage current generation.

Assuming the input DC voltage is set at 200V, the parasitic ground capacitance is 100 nF, and the semiconductor switches operate at a switching frequency of 10 kHz. Fig. 8–(a) to Fig. 8–(c) show the CMV and leakage currents of the BIH6 topology using PWM types I, II, and III as presented in [68], with a four-level output voltage and a maximum level of 400V.

Table 3. Simulation parameters for PSIM simulation

Parameters	Value
Grid	$220V_{rms}$ / 50 Hz
Switching Frequency	10 kHz
Inductor L_1, L_2	3.5 mH
Capacitor C_1, C_2	1000 μF
Voltage V_{pv}	200 V_{dc}
C_{pv}	100 nF

For PWM type I, the CMV fluctuates around 100V, but at 0.01s, a sharp spike up to 200 V occurs, causing an instant surge in leakage current i_{CM} In contrast, with PWM types II and III, v_{CM} fluctuates steadily around 100V, resulting in similar leakage current behavior in both cases. Overall, in all three traditional PWM methods, leakage current still exists and negatively affects system performance.

Fig. 8–(d) shows that the proposed modulation technique maintains the CMV at a constant value of 100V throughout the entire switching cycle. As a result, the leakage current is almost completely eliminated compared with conventional modulation methods, which is consistent with the theoretical analysis presented earlier.

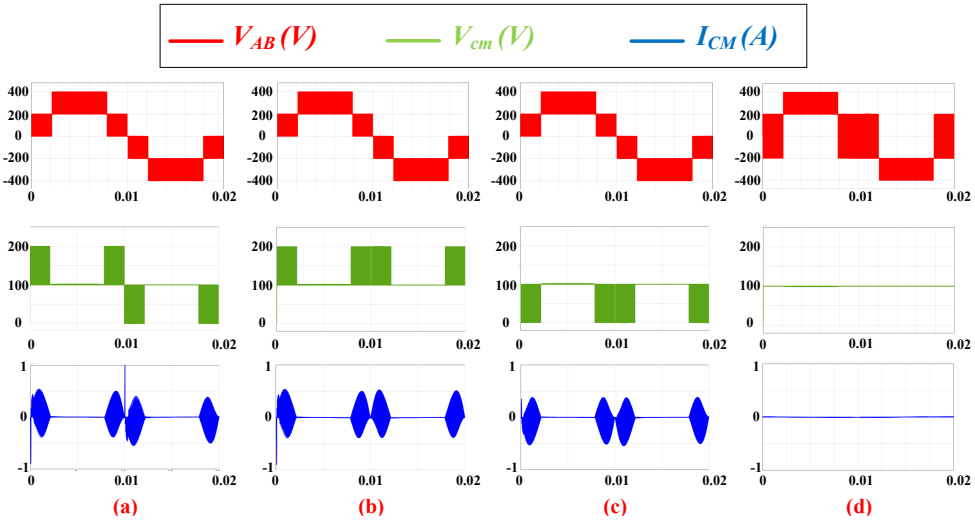


Fig. 8. Simulation results with $M_a = 1$: (a) PWM Type I (b) PWM Type II c) PWM Type III d) BIH6 inverter with the proposed PWM method

Moreover, with a modulation index $M_a < 0.5$, the simulation results in Fig. 9 show that the previous modulation methods from Fig. 9–(a) to Fig. 9–(b) still cause CMV to fluctuate throughout

the entire operating cycle, with a fluctuation amplitude of around 100V. As the modulation index decreases, this variation leads to a significant increase in leakage current.

However, with the newly proposed modulation technique applied to the BIH6 inverter, as illustrated in Fig. 9–(c) to Fig. 9–(d), this issue is significantly improved. The method maintains the common-mode voltage v_{CM} at a constant value of 100V, preventing any increase in leakage current compared with conventional modulation strategies. This demonstrates that the BIH6 inverter can operate stably across the full modulation range from 0 to 1, thereby extending its applicability under various operating conditions.

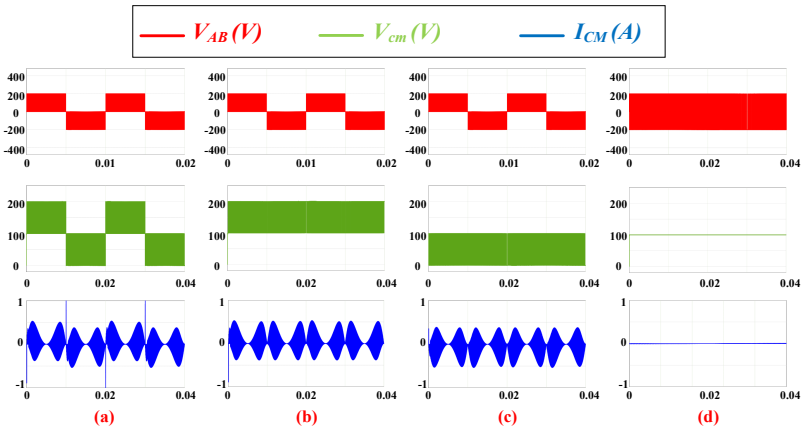


Fig. 9. Simulation Results with $M_a = 0.5$: (a) PWM Type I (b) PWM Type II c) PWM Type III d) BIH6 Inverter with the proposed PWM method

Fig. 10 illustrates the behavior of the system when V_{dc} varies from 100V to 200V and a mismatch between the inductors L_1 and L_2 is present, it can be observed that the amplitude of the CMV remains almost unchanged. The appearance of a small leakage current is consistent with practical operating conditions, since it is nearly impossible for L_1 and L_2 to be perfectly identical in real implementations. These results indicate that the LT-PWM technique is able to maintain a stable CMV across the entire V_{dc} variation range, thereby improving the leakage current behavior.

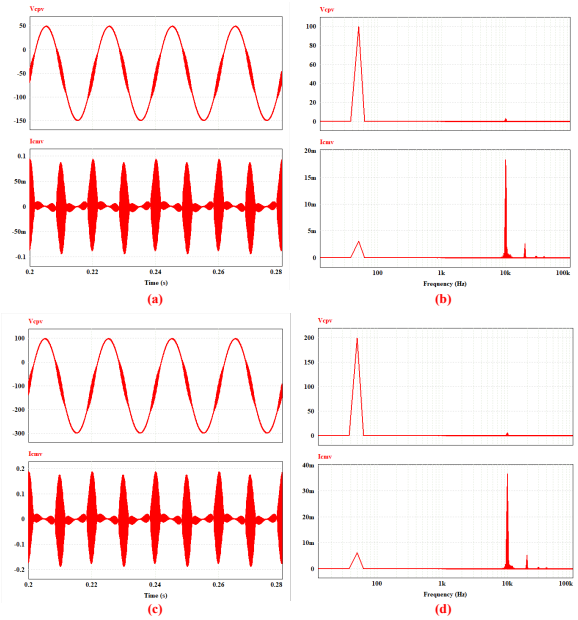


Fig. 10. Simulation results of the parasitic capacitor voltage and leakage current under the proposed method when the inductances L_1 and L_2 are mismatched. From top to bottom: (a, c) parasitic capacitor voltage and leakage current; (b, d) FFT spectrum of the parasitic capacitor voltage and FFT of the leakage current. (a, b) $V_{dc} = 100V$; (c, d) $V_{dc} = 200V$

Although a stable CMV is essential for reducing leakage current, the actual leakage current still increases slightly as V_{dc} rises. This demonstrates that leakage current is not determined solely by the CMV, but also influenced by other factors such as the parasitic capacitance C_{pv}, the mismatch between the inductors, and the harmonic distortion of the grid voltage. When a small mismatch exists between L_1 and L_2, a portion of the differential-mode voltage v_{DM} is coupled into the common-mode branch, producing a small leakage current even when the CMV is held constant.

The frequency spectra further show that the dominant leakage current components are concentrated at the grid frequency, with almost no sideband harmonics caused by CMV fluctuations. This confirms that the LT-PWM method significantly mitigates the switching induced contribution to leakage current. Overall, both simulation and experimental results validate that LT-PWM maintains a stable CMV under varying V_{dc}, while keeping the leakage current within the safety limits required for grid-connected PV systems.

Table 4 presents a comparison between the proposed LT-PWM technique and the conventional Full-State PWM method applied to the BIH6 inverter. The results indicate that the conventional approach produces a CMV level of V_{dc} and a leakage current i_{CM} of less than 100 mA. In contrast, the LT-PWM technique maintains the CMV with almost no fluctuation and reduces the leakage current to below 10 mA. These results demonstrate the effectiveness of the proposed method in controlling and significantly mitigating leakage current to a safer level for grid-connected PV systems.

Table 4. Comparison of the Proposed Method with Previous PWM Techniques for the BIH6 Inverter

PWM Method	CMV Ripple	Leakage Current	THD %
Full-State PWM [68]	$V_{dc}/2$	<100mA	<3%
Proposed	0	<10mA	<5%

Fig. 11 presents the efficiency comparison of the inverter when using the proposed LT-PWM technique and the conventional Full-State PWM method across output power levels ranging from 300 W to 1000 W. It can be observed that the efficiency of the proposed method increases with the load power, reaching approximately 96.5% at 800 W before slightly decreasing at 1000 W.

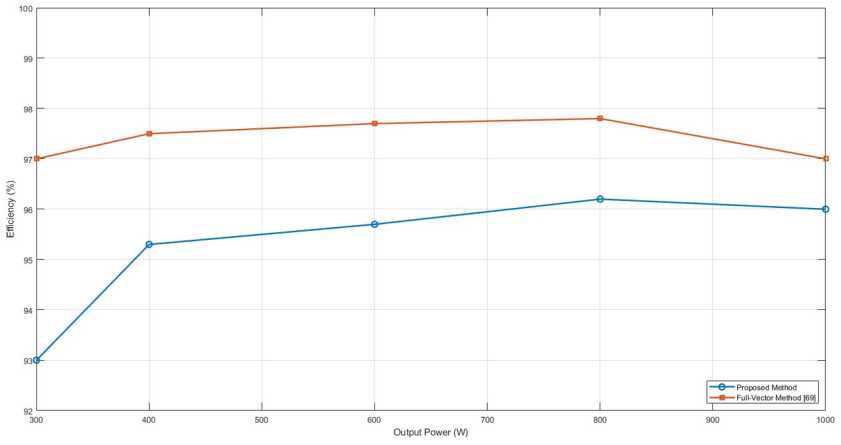


Fig. 11. Efficiency comparison between the proposed LT-PWM method and the conventional Full-State PWM

Compared with the Full-State PWM method, the LT-PWM technique exhibits a lower efficiency by approximately 1 to 1.5% over the entire power range. This reduction is primarily due to the elimination of one switching state in the proposed method, which decreases the number of output voltage levels and results in slightly higher harmonic content under certain operating conditions, thereby increasing losses in the power stage. Additionally, the mismatch between the inductors and various parasitic components in the experimental setup further contribute to the overall efficiency reduction.

The simulation model used to evaluate the grid connected operation of the BIH6 inverter under varying power conditions is illustrated in Fig. 12. At $t = 0.3s$, the active power P is increased from 500 W to 1 kW, and at $t = 0.3s$, the reactive power Q is increased to 500 Var to assess the inverter's dynamic response with the proposed control method. The results indicate that the system achieves a fast transient response with a settling time of approximately 0.25s, confirming the effectiveness of the proposed single phase grid synchronization control technique.

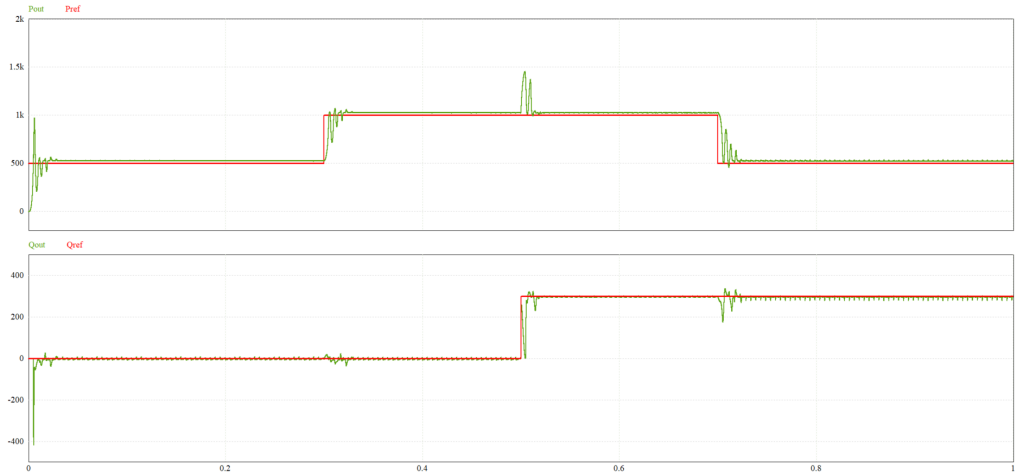


Fig. 12. Dynamic response of active and reactive power

As observed in Fig. 13, after the inverter reaches the steady state condition, the grid current waveform remains nearly sinusoidal and stable during the power transition periods. This confirms that the proposed control strategy is capable of maintaining high current quality even under varying output power conditions.

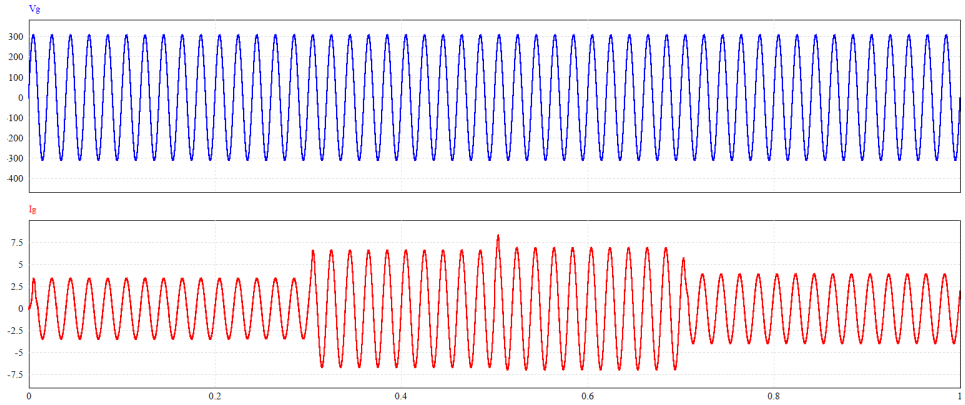


Fig. 13. Waveforms of grid voltage and current during power variation

The experimental results presented in this section aim to demonstrate the feasibility and effectiveness of the proposed leakage current reduction method. The key components of the system are listed in Table 5. The experiment was conducted on a 500W BIH6 inverter, as shown in Fig. 14. The experimental results confirm that the proposed control method significantly reduces leakage current, validating the effectiveness of this solution.

Table 5. Components of the 500W inverter prototype

Parameters	Value
Grid	110Vrms/50Hz
Inductor filter	$L_1 = L_2 = 3.5\ mH$
Capacitances	$C_1 = C_2 = 3300uF$
Switches / Diodes	60N100×7 / RHRG75120×2

A direct current (DC) source can be used as an alternative to the PV source to supply power to the inverter. To achieve an output voltage of 110 V_{rms}, the BIH6 inverter is controlled using the three-level pulse width modulation (LT-PWM) technique, operating at a carrier frequency of 10 kHz with a modulation index of $M_a = 0.8$. Under these conditions, the input DC voltage is set to $V_{dc} = 100V$. Thanks to the voltage doubling structure of the BIH6 inverter, the DC-link voltage is boosted to 200V. Fig. 15–(a) illustrates the input DC voltage and the voltages across capacitors C_1 and C_2. The voltage V_{dc} is evenly distributed across the two capacitors, with a ripple voltage of approximately 1V during the entire switching cycle.

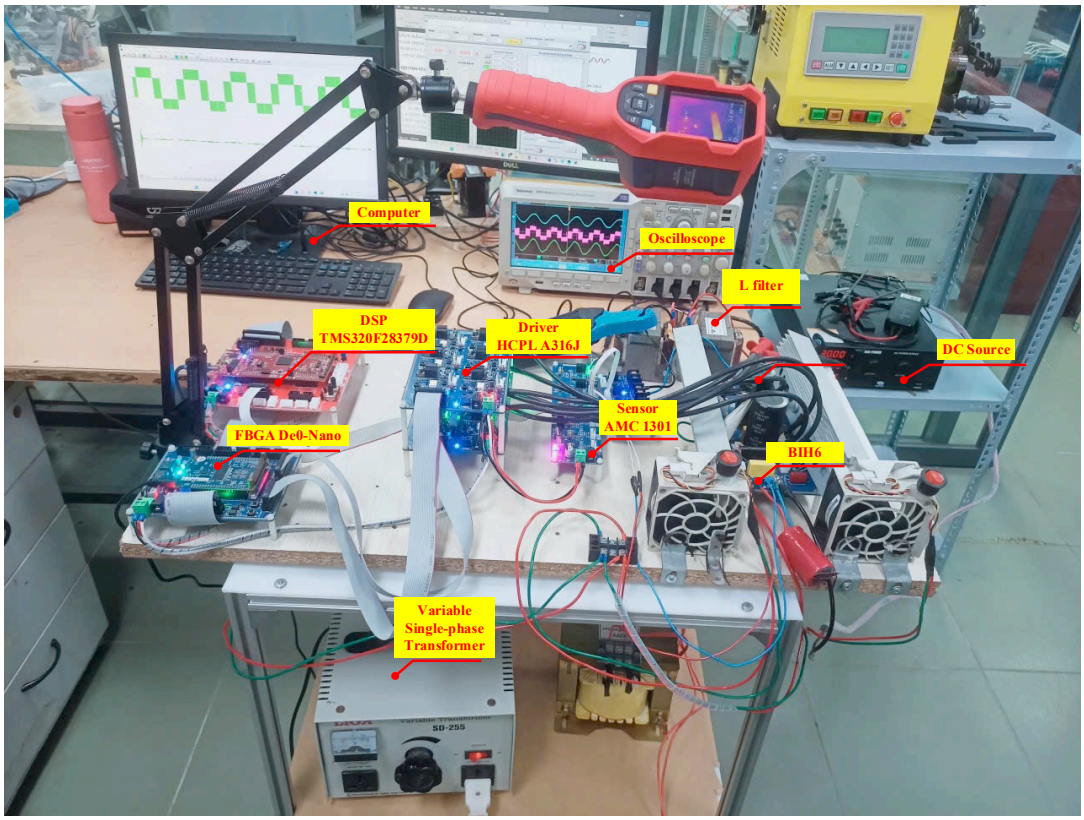


Fig. 14. Photograph of the laboratory prototype model

The inverter is controlled to inject grid current under three operating modes: in-phase Fig. 15–(b), leading-phase Fig. 15–(c), and lagging-phase Fig. 15–(d). The results confirm that the inverter maintains stable operation, proper grid current tracking, and high efficiency across all operating modes with different power factor values. The THD of the injected current remains below 5%, demonstrating that the LT-PWM strategy provides reliable control performance under various reactive power conditions.

However, it is also observed that at very low modulation indices, particularly when $M_a < 0.4$, the effective number of output voltage levels decreases to only two. This reduction leads to higher harmonic distortion because the switching states become insufficient to synthesize a multi-level waveform. Therefore, the proposed LT-PWM technique operates most effectively within the practical modulation range of $M_a > 0.5$, where four-level output behavior is maintained, ensuring low THD and stable grid current quality.

The sum of the voltage waveforms v_{AN} and v_{BN} indicates that the CMV is maintained constant at $V_{dc}/2$. Fig. 15–(e) illustrates the system's CMV, where the sum of $V_{an} + V_{bn}$ yields a value of 50 V. Fig. 15–(f) shows the voltage waveform across the parasitic capacitor C_{pv}. The observation reveals that the leakage current is almost completely suppressed, with only a very small remaining value the RMS leakage current is approximately 9 mA.

The experimental results in Fig. 16–(a) and Fig. 16–(b) show the parasitic capacitor voltage v_{CPV} and the leakage current i_{CM} under practical operating conditions of the BIH6 inverter. It can be observed that the waveform of v_{CPV} remains stable in both cases, demonstrating strong consistency between the simulation and experimental results regarding the common-mode voltage characteristics.

The experimental leakage current i_{cm} contains more high-frequency noise compared with the simulation, mainly due to PCB parasitics, hardware layout, and measurement interference. However, the leakage current magnitude does not increase significantly and remains within the safety limits, consistent with the leakage current reduction trend observed in the simulation.

The frequency spectra of v_{CM} shown in the lower part of the figure indicate that the switching-frequency components appear only at very low amplitudes and do not generate significant sidebands that could affect the leakage current. This confirms that the LT-PWM technique effectively suppresses CMV fluctuation even in real operating environments, where parasitics and noise levels are inherently higher than in the idealized simulation model.

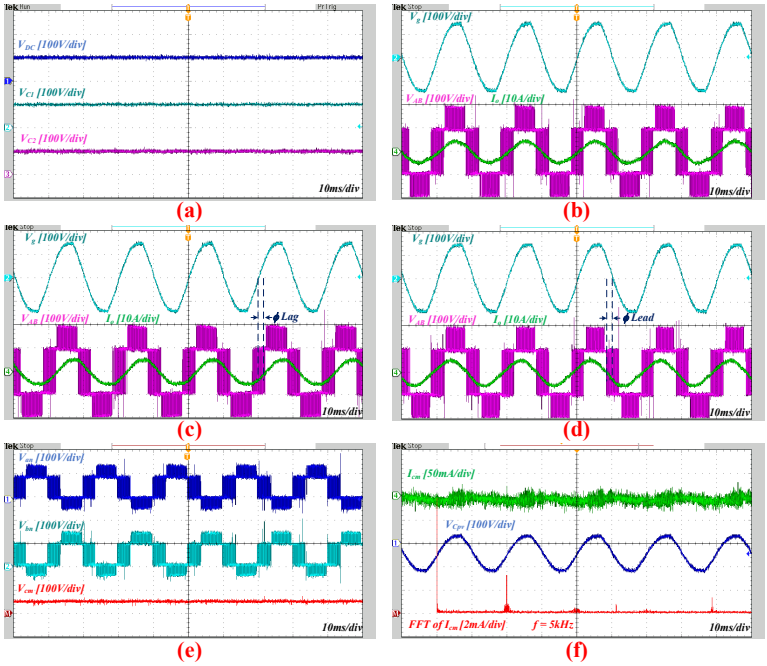


Fig. 15. Experimental waveforms: (a) Voltages of the DC input Vdc and voltages of the floating capacitors C_1 and C_2; (b) UPF operation; (c) Lagging PF operation; (d) Leading PF operation; (e) The voltage waveforms v_{AN}, v_{BN}, and v_{CM}; (f) The leakage current waveform and the voltage across the capacitor C_{pv}

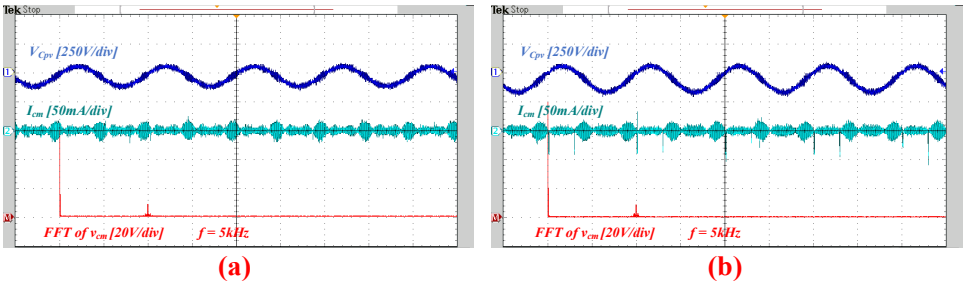


Fig. 16. Waveforms of stray capacitor voltage v_{CPV} and leakage current i_{CM} : (a) $V_{dc} = 100V$; (b) $V_{dc} = 200V$

The total harmonic distortion (THD) of the grid current and voltage is illustrated in Fig. 17. The results indicate that the THD values of both current and voltage remain low across the entire power range from 100 W to 500 W. In particular, the current THD consistently stays below 5%, confirming

that the proposed control strategy effectively improves the quality of the injected grid current and meets the grid compliance requirements.

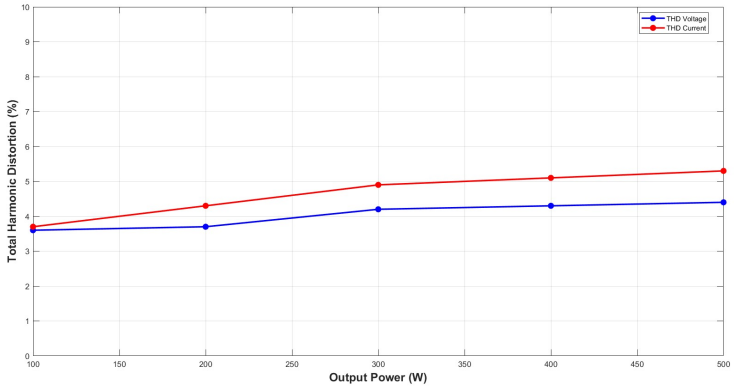


Fig. 17. THD of current and voltage in grid-connected mode

The power loss calculation results obtained from PSIM software are illustrated in Fig. 18, showing the power loss distribution among the circuit components when the inverter operates at 500 W. The results indicate that the total power loss is approximately 50 W, accounting for about 10% of the input power. The analysis reveals that the major losses occur in the power switches S_1, S_2, and S_3, as they operate in switching mode throughout the entire cycle, while the losses in the diodes are negligible. This confirms that the efficiency of the BIH6 inverter is strongly influenced by the conduction and switching characteristics of the semiconductor devices. Table 6 presents a comparative analysis between the proposed method and several recently published approaches. Notably, the proposed LT-PWM technique demonstrates superior performance in terms of leakage current reduction as well as its inherent capability to achieve voltage doubling, outperforming the existing methods according to the data summarized.

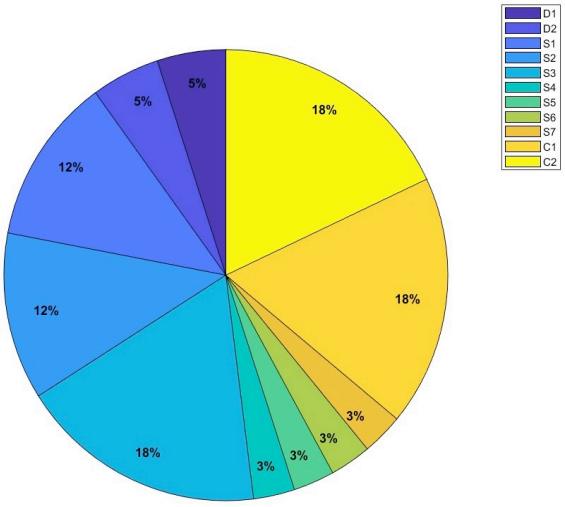


Fig. 18. Power loss analysis of the inverter operating at 500 W

Table 6. Comparison of existing solutions with proposed method

References	Semiconductors		Voltage Levels	Leakage Current	Efficiency%	THD%	Boosting
	Switches	Diodes					
[72]	7	0	3	15	96.3	N/A	yes
[72]	9	1	5	12.8	97	1.29	yes
[73]	7	2	5	12	97.98	4.57	yes
[74]	6	0	N/A	0	96.6	3	No
LT-PWM	7	2	4	10	95	4	yes

N/A – Not Available

5. Conclusion

This paper presented an LT-PWM modulation technique for the BIH6 inverter to suppress CMV oscillations and significantly reduce leakage current in transformerless grid connected PV systems. By eliminating the two zero switching states responsible for CMV transitions, the proposed method maintains a constant CMV at V_{dc} and reduces the leakage current to below 10mA at $V_{dc} = 100V$, which is nearly ten times lower than that of conventional PWM. The leakage current also remains within safe limits even when V_{dc} increases to 200V or even when the inductor mismatch is small, demonstrating strong robustness under practical conditions. The output THD stays below 5%, and the inherent voltage doubling capability of the BIH6 inverter is preserved without requiring an additional DC-DC stage. An efficiency of approximately 96.5% at 800W confirms an acceptable trade off between CMV reduction and switching state simplification. However, the LT-PWM technique presents certain limitations, particularly at low modulation indices ($M_a < 0.5$), where the effective number of voltage levels decreases and the THD tends to increase. Moreover, switching losses at higher power ratings have not yet been fully assessed. Future research will focus on optimizing the modulation strategy to further reduce losses, validating the approach on higher power prototypes, integrating it with advanced multilevel inverter structures, and developing adaptive control methods to enhance system robustness under real world grid disturbances.

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