IJRCS

International Journal of Robotics and Control Systems
Vol. 6, No. 1, 2026, pp. 243-261
ISSN 2775-2658
http://pubs2.ascee.org/index.php/ijrcs

ASCEE

A Three Phase Switched-Capacitor Based Boost Ten-Switch Inverter for Common Mode Voltage Reduction

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ARTICLE INFO

Article history
Received November 07, 2025
Revised January 14, 2026
Accepted January 27, 2026

Keywords
Common-Mode Voltage;
Ten-Switch Inverter;
Space-Vector Pulse-Width Modulation;
Switch-Capacitor

ABSTRACT

This paper proposes a three-phase ten-switch inverter topology integrating a switched-capacitor voltage doubler to achieve both voltage boosting and effective common-mode voltage (CMV) reduction. Unlike conventional three-phase inverters, which suffer from limited voltage gain and large CMV fluctuations leading to increased leakage current and electromagnetic interference, the proposed configuration introduces a voltage-doubling stage that boosts the DC-link voltage to twice the input level while maintaining inherent capacitor voltage self-balancing without additional sensors or complex control. The ten-switch structure provides flexible switching control that actively suppresses DC-link voltage fluctuations and significantly reduces CMV amplitude. A dedicated space vector pulse width modulation strategy employing a single zero vector, combined with a logic-based switching function, is developed to confine CMV variation within a narrow range of 1/6 to 1/3 of the DC-link voltage. By constraining CMV fluctuation, leakage current is reduced, thereby improving operational safety in transformerless systems, while the voltage stress across power semiconductor devices remains inherently limited. Comprehensive theoretical analysis, detailed operational principles, PSIM simulations, and experimental validations confirm effective CMV suppression, good conversion efficiency, balanced capacitor voltages, and practical feasibility, demonstrating that the proposed inverter is a promising and cost-effective solution for high-performance photovoltaic and motor-drive applications.

1. Introduction

Three-phase inverters are widely adopted in both industrial and residential applications, ranging from induction motor drive systems to grid-connected systems and DC-AC power conversion. However, common-mode voltage is a critical issue that must be addressed in three-phase inverters employing high-frequency switching semiconductor devices under pulse width modulation (PWM) techniques [1]-[5]. CMV can lead to severe problems, including electromagnetic interference (EMI) [6]-[9], leakage currents in transformerless grid-connected photovoltaic (PV) systems [10]-[12], and

leakage currents in motor drives [13]-[16]. Specifically, EMI affects nearby electronic equipment and can cause misoperation of switching signals in inverters [17]. In PV systems, a parasitic capacitance exists between the PV panel and the grid ground. The interaction between this parasitic capacitance and the CMV generates voltage oscillations and results in leakage currents, which increase energy losses and reduce the reliability of PV inverters [18]-[23]. Similarly, in electric drives, parasitic capacitance in motors [24]-[28] or magnetic field asymmetries due to mechanical imperfections or uneven stator winding distributions can create significant problems [29]. When combined with CMV, these factors induce leakage currents that negatively affect motor performance, increase power losses, and reduce motor lifespan [30]-[35].

To mitigate the impact of CMV, passive filter solutions are often implemented at the inverter output by adding components such as common-mode chokes or inductor-capacitor-resistor circuits [36]-[40]. Although these methods are effective, they significantly increase system cost and size [41]-[43]. As a result, recent research has shifted focus toward enhancing PWM techniques. While traditional sine pulse-width modulation (SPWM) and space-vector pulse-width modulation (SVPMW) methods have proven effective for inverter control, they offer limited capability in suppressing CMV. Therefore, various advanced PWM strategies have been proposed to reduce CMV fluctuation, such as Active Zero-State PWM (AZPWM) [44], [45], Near-State PWM (NSPWM) [46], Remote-State PWM (RSPWM) [47], and Hybrid Space Vector Pulsewidth Modulation Synthesis (HSVPWMS) [48]. These approaches have demonstrated good effectiveness in reducing both the amplitude and frequency of CMV. However, they often result in increased total harmonic distortion in the output current (THDi) and elevated voltage stress [49], [50] on the output filter.

Beyond passive filters and PWM strategies, there is a growing interest in improving inverter topologies by incorporating additional semiconductor devices in conjunction with suitable modulation techniques. A seven-switch (H7) inverter topology, combined with a modified PWM (MDPWM) strategy for leakage current suppression in transformerless PV systems, was proposed in [51]. However, the H7 configuration maintains a continuous conduction path between the inverter and the PV system, limiting its leakage current mitigation capability. An H7 topology [52] has been introduced to mitigate CMV. However, the inclusion of six diodes and one additional semiconductor switch increases both the conduction losses and the overall system cost. To further enhance the suppression of common-mode voltage, the eight-switch (H8) configuration [53] incorporates only two auxiliary switches, thereby reducing the overall circuit footprint compared to the H8 configuration in [54], which employs two additional DC-link switches together with a capacitive divider and two clamping diodes. Although the H8 topology in [54] can significantly reduce the CMV amplitude, its applicability in high power systems is limited due to the low modulation index ($Mi < 0.5$). The modulation index is defined as $Mi = \sqrt{3}V_m/V_{PN}$, where V_m is the amplitude of reference voltage, and V_{PN} is DC-link voltage. To address this, the ten-switches (H10) structure was proposed in [55], employing the H10 including two isolation switches and an integrated clamping circuit within a conventional three-phase inverter. However, the use of clamping capacitors leads to increased system cost. To overcome this limitation, an enhanced version derived from the H8 configuration was developed [56], known as the NCH10 topology [57], which arranges ten switches strategically without the need for clamping capacitors. Although this structure still achieves CMV reduction, its overall efficiency remains limited due to frequent operation in zero vector states.

In this paper, a novel three-phase inverter topology employing ten semiconductor switches (SCB^{2}TSI) is proposed, combining a switched-capacitor voltage doubler stage [58]-[63] with a configuration consisting of ten semiconductor switches. Based on this topology, a dedicated PWM method is developed that utilizes only one zero vector V_7 (111), along with a logic function to control the switching states. Compared with existing H8- and H10-based inverter structures, the proposed SCB^{2}TSI topology offers several practical advantages. The H8 configurations primarily focus on CMV reduction but do not provide inherent voltage-boosting capability, which limits their applicability in low-voltage DC-source systems. The H10 topology can further suppress CMV. However, they often rely on clamping capacitors or additional auxiliary circuits, leading to increased

component count and more complex voltage-balancing requirements. In contrast, the proposed SCB^{2}TSI integrates a switched-capacitor voltage doubler that simultaneously achieves DC-link voltage boosting and CMV reduction while maintaining natural capacitor voltage self-balancing. Moreover, the device voltage stress in the proposed topology is inherently limited to the input DC voltage, enhancing reliability and suitability for practical implementation. These features distinguish the proposed SCB^{2}TSI from existing ten-switch inverter configurations and highlight its advantages in terms of performance and engineering feasibility. Simulation and experimental results confirm that the proposed structure significantly reduces CMV amplitude, maintaining voltage fluctuation at approximately 16.66% of the DC-link voltage. This contributes to effective leakage current suppression in transformerless PV systems and electric drive applications.

2. Proposed Topology and the Operation Principle

The proposed SCB^{2}TSI topology is realized by integrating a switched-capacitor voltage doubler (SCVD) network with an eight-switch inverter stage. The SCVD network comprises two diodes (D_a, D_b) and two power switches (S_U, S_D), which are alternately operated to boost the input DC voltage (V_{DC}). The eight-switch inverter is augmented with two auxiliary switches S_7 and S_8 to enhance modulation flexibility and enable effective common-mode voltage control. The detailed circuit configuration of the proposed topology is shown in Fig. 1. The subsequent sections present the operating principles for each mode and analyze the associated modulation strategies to achieve high-performance CMV suppression.

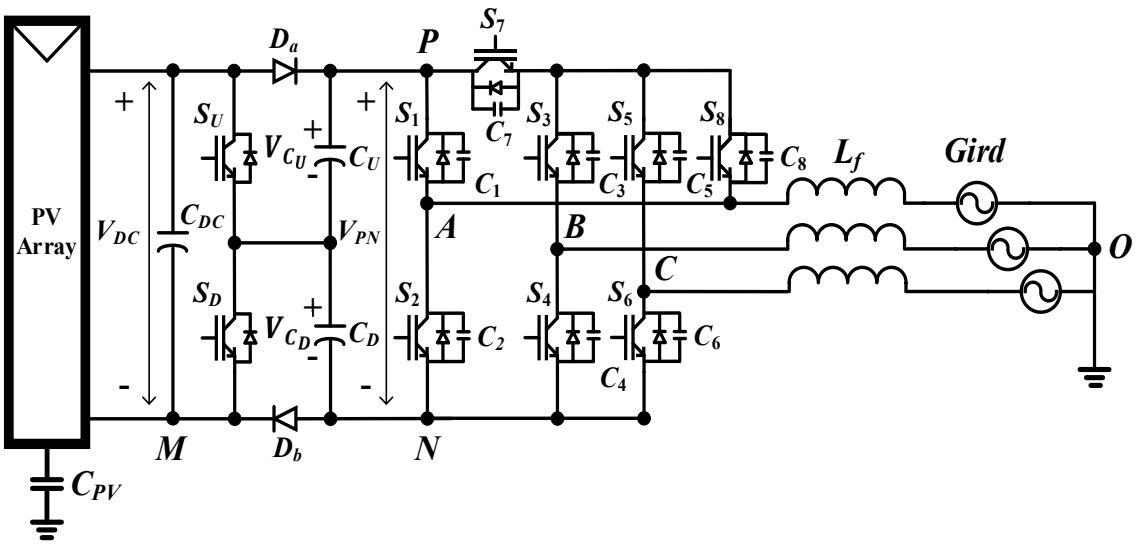


Fig. 1. Topology of the proposed SCB^{2}TSI

2.1. Operation Mode of SCB^{2}TSI Structure

Unlike the conventional SVPWM strategy employed in three-phase inverters which utilizes eight switching states (six active states and two zero states), the proposed modulation strategy in this study adopts a single zero vector in combination with a logic-based function to generate seven switching states. This set of states includes both active and zero states, determined through a logic function with the objective of reducing the CMV and improving the output voltage quality. Table 1 presents the detailed switching configurations corresponding to each operating state of the semiconductor switches in the proposed inverter topology.

As presented in Fig. 2 a, Fig. 2 c, and Fig. 2 e, operating states 1, 3, and 5 correspond to the condition in which switch S_U is turned "ON" while switch S_D is turned "OFF". During these states, capacitor C_D undergoes a charging process, whereas capacitor C_U discharges its stored energy to the load. Conversely, Fig. 2 b, Fig. 2 d, and Fig. 2 f illustrate operating states 2, 4 and 6 in which S_U is

"OFF" and S_D is "ON". In this mode of operation, capacitor C_D discharges and C_U is charged. Throughout these states, the inverter switches S_1 to S_6 operate in the same manner as those in a conventional three-phase inverter, except during the application of the zero vector. Furthermore, the proposed topology integrates two auxiliary switches, S_7 and S_8, which are designed to operate in a complementary fashion.

Table 1. Switching-state-based operation modes of the proposed inverter

Modes	Switch								Output leg volage			V_{CMV}
	S_1	S_2	S_3	S_5	S_7	S_8	S_U	S_D	V_{AN}	V_{BN}	V_{CN}	
State 1	ON	OFF	OFF	OFF	ON	OFF	ON	OFF	V_{PN}	0	0	$V_{PN}/3$
State 2	ON	OFF	ON	OFF	ON	OFF	OFF	ON	V_{PN}	V_{PN}	0	$V_{PN}/6$
State 3	OFF	ON	ON	OFF	ON	OFF	ON	OFF	0	V_{PN}	0	$V_{PN}/3$
State 4	OFF	ON	ON	ON	ON	OFF	OFF	ON	0	V_{PN}	V_{PN}	$V_{PN}/6$
State 5	OFF	ON	OFF	ON	ON	OFF	ON	OFF	0	0	V_{PN}	$V_{PN}/3$
State 6	ON	OFF	OFF	ON	ON	OFF	OFF	ON	V_{PN}	0	V_{PN}	$V_{PN}/6$
State 7*	OFF	OFF	ON	ON	OFF	ON	OFF	ON	V_{PN}	V_{PN}	V_{PN}	-

* The value of CMV depends on the capacitance values of C_1 through C_8 and the switching states of the power devices. This relationship will be analyzed in detail in the following section

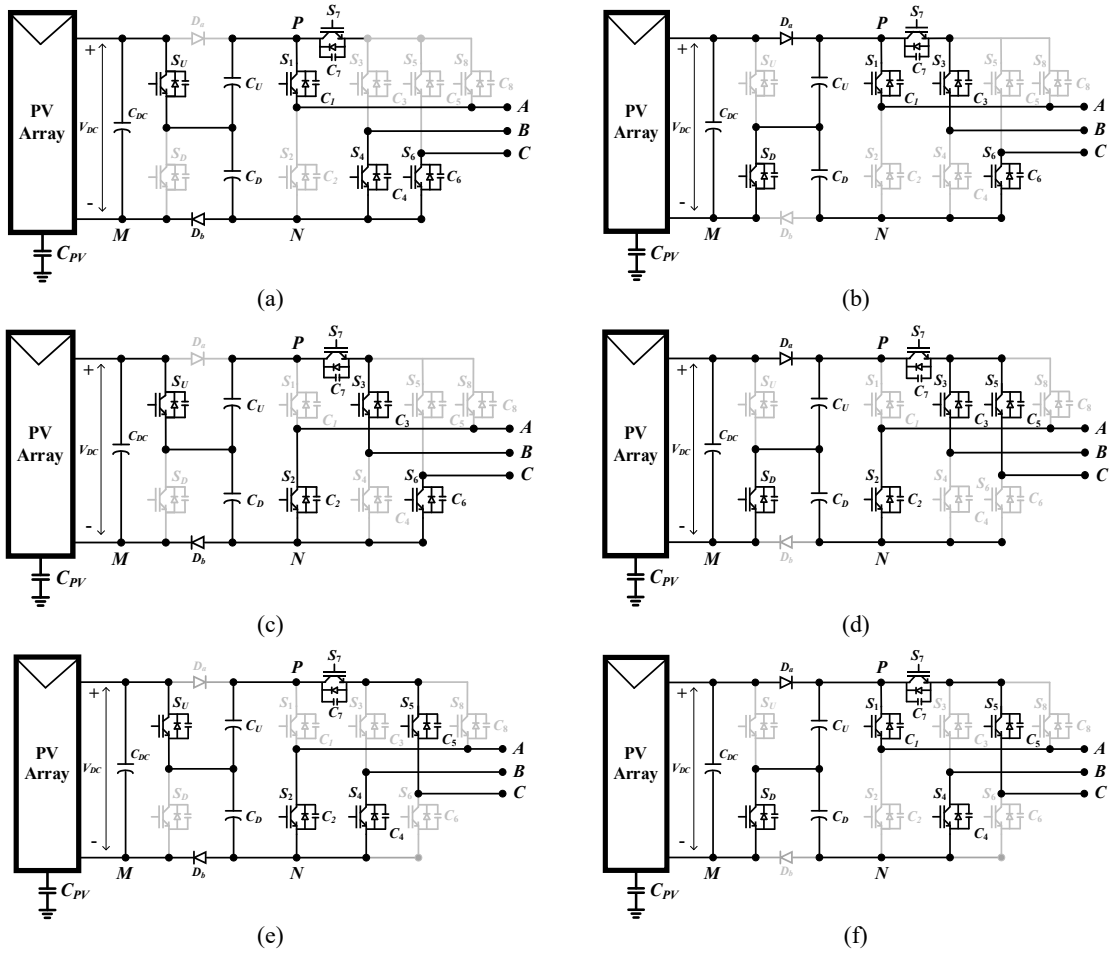


Fig. 2. Configuration of the proposed SCB^{2}TSI for the active vector states: (a) State 1 (100), (b) State 2 (110), (c) State 3 (010), (d) State 4 (011), (e) State 5 (001), and (f) State 6 (101)

Specifically, during active states, if S_7 is turned "ON", then S_8 is turned "OFF", and vice versa, ensuring proper control over the switching sequences and reducing the CMV fluctuations. The zero state, illustrated in Fig. 3, is characterized by switches S_1, S_2, S_4, S_6, S_7 and S_U being turned "OFF", while switches S_3, S_5, and S_8 are turned "ON", forming a current path through the output filter inductors. In this state, capacitor C_U is charged, whereas capacitor C_D is discharged. Since both

capacitors CU and CD alternately undergo charging and discharging within each switching cycle, maintaining their voltages approximately equal to the input DC voltage requires the system to operate at a high switching frequency. A high switching frequency not only ensures voltage balancing across the capacitors but also improves the stability and overall efficiency of the inverter.

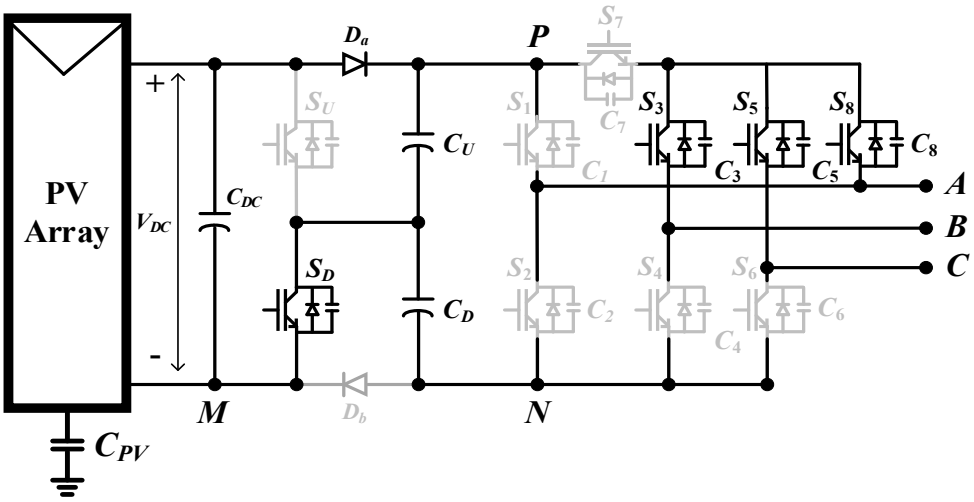


Fig. 3. Configuration of the proposed SCB^{2}TSI for zero state 7

2.2. Common-Mode Voltage Analysis Using Capacitor Model

The common-mode voltage of a three-phase inverter is defined as the average of the three instantaneous output phase voltages. In the proposed configuration, the common-mode voltage comprises two components: (i) the CMV generated by the eight-switch inverter (V_{ON}); and (ii) the voltage between point N (negative terminal of the DC-link) and point M (negative terminal of the input DC source) (V_{NM}), as show in (1). Variations in the CMV produce undesirable voltage spikes, which cause continuous charging and discharging of the parasitic capacitance between the photovoltaic (PV) module and the ground. This phenomenon results in ground leakage current, reducing energy conversion efficiency and posing potential safety risks during system operation. Therefore, controlling and mitigating CMV fluctuations is crucial to maintain system stability and operational efficiency. A simple equivalent CMV model for analytical purposes is shown in Fig. 4.

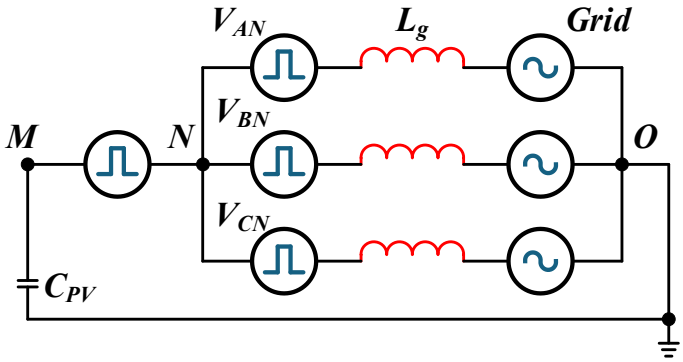


Fig. 4. Common-mode equivalent circuits of the SCB^{2}TSI for CMV analysis

The CMV of the proposed SCB^{2}TSI is determined by the following equation:

$$V_{CMV} = V_{ON} + V_{NM} \tag{1}$$

Where V_{NM} depends on the switching state of S_D. Specifically, $V_{NM} = -V_{CD}$ when S_D is turned "ON", and $V_{NM} = 0$ when S_D is turned "OFF". At this instant, the voltage between point N (negative terminal of the DC-link) and point O, denoted as V_{ON}, is determined by (2):

$$V_{ON} = \frac{V_{AN} + V_{BN} + V_{CN}}{3} \tag{2}$$

In the seventh state, nodes A, B and C are shorted together because switches S_3, S_5 and S_8 of the proposed SCB²TSI are turned "ON". In this state, V_{AN}, V_{BN} and V_{CN} are equal. When analyzing the CMV, the influence of the parasitic capacitances of the semiconductor switches must be considered,

As they can affect the output voltage characteristics. In the zero-vector modulation process, the three active vectors V_2, V_4, and V_6 are transitioned to the zero vector V_7. Although these switching transitions do not generate a voltage across the load, they cause instantaneous variations in the CMV due to changes in switching states and the influence of parasitic elements, particularly the parasitic capacitances of the switches. The transitions $V_2 \rightarrow V_7$, $V_4 \rightarrow V_7$ and $V_6 \rightarrow V_7$ are analyzed in detail to evaluate their CMV impact. Based on the results, suitable parasitic capacitance values for the switches are proposed to ensure that CMV fluctuations remain within the allowable limits of the proposed inverter. The frequency-domain analysis of the three cases is presented below.

Case 1: When vector V_2 is transitioned to vector V_7. Using the Laplace transform with the initial capacitor voltages in state V_2 (110), as shown in Fig. 5 a. By applying Kirchhoff's voltage and current laws in the directions indicated in Fig. 5 a, the following equation (3) is obtained:

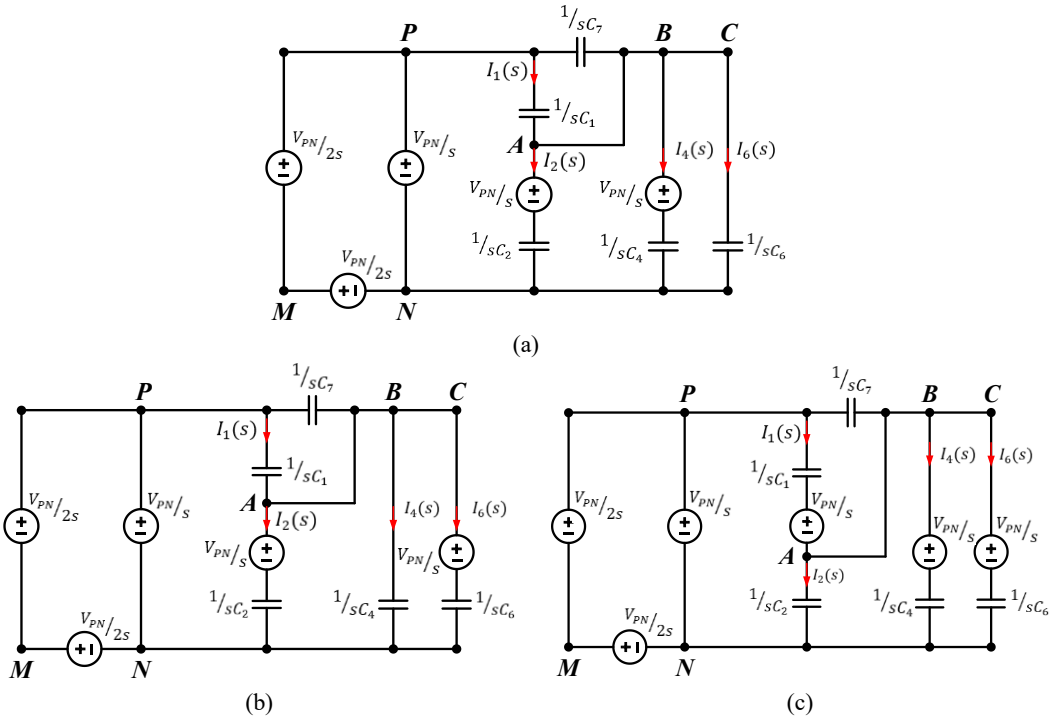


Fig. 5. Complex frequency-domain model of the proposed inverter in the (111) state: (a) Switching transition from vector V_2 to vector V_7, (b) Switching transition from vector V_6 to vector V_7, and (c) Switching transition from vector V_4 to vector V_7

$$\begin{bmatrix} 0 & 0 & \frac{1}{s.C_4} & \frac{-1}{s.C_6} \\ 0 & \frac{1}{s.C_2} & \frac{-1}{s.C_4} & 0 \\ \left(\frac{1}{s.C_1}+\frac{1}{s.C_7}\right) & \frac{-1}{s.C_7} & \frac{-1}{s.C_7} & \frac{-1}{s.C_7} \\ \frac{1}{s.C_1} & \frac{-1}{s.C_2} & 0 & 0 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_4 \\ I_6 \end{bmatrix} = \begin{bmatrix} -\frac{V_{PN}}{s} \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{3}$$

$$\begin{cases} I_1 = \dfrac{C_1.C_6.V_{PN}}{C_1+C_2+C_4+C_6+C_7} \\ I_2 = \dfrac{-C_2.C_6.V_{PN}}{C_1+C_2+C_4+C_6+C_7} \\ I_4 = \dfrac{-C_4.C_6.V_{PN}}{C_1+C_2+C_4+C_6+C_7} \\ I_6 = \dfrac{-C_6.V_{PN}.(C_1+C_2+C_4+C_7)}{C_1+C_2+C_4+C_6+C_7} \end{cases} \quad (4)$$

The voltage $V_{AN}(s)$ are expressed as in (5):

$$V_{AN}(s) = \frac{-C_6.V_{PN}}{s.(C_1+C_2+C_4+C_6+C_7)} + \frac{V_{PN}}{s} \quad (5)$$

$$V_{AN}(s) = V_{BN}(s) = V_{CN}(s) \quad (6)$$

The voltage $V_{NM}(s)$ is expressed as in (7):

$$V_{NM}(s) = \frac{-V_{PN}}{2.s} \quad (7)$$

The CMV of the SCB^{2}TSI is expressed as in (8):

$$V_{CMV}(s) = [V_{AN}(s) + V_{NM}(s)] \quad (8)$$

Taking the inverse Laplace transform of (8) and using linearity yields the time-domain expression in (9):

$$V_{CMV} = \frac{-C_6.V_{PN}}{C_1+C_2+C_4+C_6+C_7} + \frac{V_{PN}}{2} \quad (9)$$

By selecting the capacitor values as $C_7 = C_8 = 2C$ and $C_1 = C_2 = C_3 = C_4 = C_5 = C_6 = C$. The CMV of the proposed inverter at state 7, when vector V_2 is transitioned to vector V_7 is $V_{CMV} = V_{PN}/3$.

Case 2: When vector V_6 is transitioned to vector V_7. Using the Laplace transform with the initial capacitor voltages in state V_6 (101), as shown in Fig. 5 b. By applying Kirchhoff's voltage and current laws in the directions indicated in Fig. 5 b, the following equation (10) is obtained:

$$\begin{bmatrix} 0 & 0 & \frac{1}{s.C_4} & \frac{-1}{s.C_6} \\ 0 & \frac{1}{s.C_2} & 0 & \frac{-1}{s.C_6} \\ \left(\frac{1}{s.C_1}+\frac{1}{s.C_7}\right) & \frac{-1}{s.C_7} & \frac{-1}{s.C_7} & \frac{-1}{s.C_7} \\ \frac{1}{s.C_1} & \frac{1}{s.C_2} & 0 & 0 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_4 \\ I_6 \end{bmatrix} = \begin{bmatrix} \frac{V_{PN}}{s} \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (10)$$

$$\begin{cases} I_1 = \dfrac{C_1.C_4.V_{PN}}{C_1+C_2+C_4+C_6+C_7} \\ I_2 = \dfrac{-C_2.C_4.V_{PN}}{C_1+C_2+C_4+C_6+C_7} \\ I_4 = \dfrac{C_4.V_{PN}.(C_1+C_2+C_6+C_7)}{C_1+C_2+C_4+C_6+C_7} \\ I_6 = \dfrac{-C_6.C_4.V_{PN}}{C_1+C_2+C_4+C_6+C_7} \end{cases} \quad (11)$$

The voltage $V_{AN}(s)$ are expressed as in (12):

$$V_{AN}(s) = \frac{-C_4.V_{PN}}{s.(C_1+C_2+C_4+C_6+C_7)} + \frac{V_{PN}}{s} \tag{12}$$

$$V_{AN}(s) = V_{BN}(s) = V_{CN}(s) \tag{13}$$

The voltage $V_{NM}(s)$ is expressed as in (14):

$$V_{NM}(s) = \frac{-V_{PN}}{2.s} \tag{14}$$

The CMV of the SCB^{2}TSI is expressed as in (15):

$$V_{CMV}(s) = [V_{AN}(s) + V_{NM}(s)] \tag{15}$$

Taking the inverse Laplace transform of (15) and using linearity yields the time-domain expression in (16):

$$V_{CMV} = \frac{-C_4.V_{PN}}{C_1+C_2+C_4+C_6+C_7} + \frac{V_{PN}}{2} \tag{16}$$

By selecting the capacitor values as $C_7 = C_8 = 2C$ and $C_1 = C_2 = C_3 = C_4 = C_5 = C_6 = C$. The CMV of the proposed inverter at state 7, when vector V_6 is transitioned to vector V_7 is $V_{CMV} = V_{PN}/3$.

Case 3: When vector V_4 is transitioned to vector V_7. Using the Laplace transform with the initial capacitor voltages in state V_4 (011), as shown in Fig. 5 c. By applying Kirchhoff's voltage and current laws in the directions indicated in Fig. 5 c, the following equation (17) is obtained:

$$\begin{bmatrix} 0 & \frac{1}{s.C_2} & 0 & \frac{-1}{s.C_6} \\ 0 & 0 & \frac{1}{s.C_4} & \frac{-1}{s.C_6} \\ \left(\frac{1}{s.C_1}+\frac{1}{s.C_7}\right) & \frac{-1}{s.C_7} & \frac{-1}{s.C_7} & \frac{-1}{s.C_7} \\ \frac{1}{s.C_1} & \frac{-1}{s.C_2} & 0 & 0 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_4 \\ I_6 \end{bmatrix} = \begin{bmatrix} \frac{V_{PN}}{s} \\ 0 \\ \frac{-V_{PN}}{s} \\ 0 \end{bmatrix} \tag{17}$$

$$\begin{cases} I_1 = \frac{-C_1.V_{PN}.(C_4+C_6+C_7)}{C_1+C_2+C_4+C_6+C_7} \\ I_2 = \frac{C_2.V_{PN}.(C_4+C_6+C_7)}{C_1+C_2+C_4+C_6+C_7} \\ I_4 = \frac{-C_4.V_{PN}.(C_1+C_2)}{C_1+C_2+C_4+C_6+C_7} \\ I_6 = \frac{-C_6.V_{PN}.(C_1+C_2)}{C_1+C_2+C_4+C_6+C_7} \end{cases} \tag{18}$$

The voltage $V_{AN}(s)$ are expressed as in (19):

$$V_{AN}(s) = \frac{V_{PN}.(C_4+C_6+C_7)}{s.(C_1+C_2+C_4+C_6+C_7)} \tag{19}$$

$$V_{AN}(s) = V_{BN}(s) = V_{CN}(s) \tag{20}$$

The voltage $V_{NM}(s)$ is expressed as in (21):

$$V_{NM}(s) = \frac{-V_{PN}}{2.s} \tag{21}$$

The CMV of the SCB^{2}TSI inverter is expressed as in (22):

$$V_{CMV}(s) = [V_{AN}(s) + V_{NM}(s)] \tag{22}$$

Taking the inverse Laplace transform of (22) and using linearity yields the time-domain expression in (23):

$$V_{CMV} = \frac{V_{PN}.(C_4 + C_6 + C_7)}{C_1 + C_2 + C_4 + C_6 + C_7} - \frac{V_{PN}}{2} \tag{23}$$

By selecting the capacitor values as $C_7 = C_8 = 2C$ and $C_1 = C_2 = C_3 = C_4 = C_5 = C_6 = C$. The CMV of the proposed inverter at state 7, when vector V_4 is transitioned to vector V_7 is $V_{CMV} = V_{PN}/6$. Based on the analysis of the CMV at state 7 and the preceding switching states, Table 2 summarizes the corresponding CMV values for each operating state. These results directly stem from the proposed capacitor equivalent model and demonstrate how the selected capacitance ratios and switching transitions determine the CMV levels. Accordingly, the model provides a clear design reference for defining the inverter operating states and the associated modulation strategy.

Table 2. CMV for indivial operating sates

Modes	V_{NM}	V_{AN}	V_{BN}	V_{CN}	V_{CMV}
State 1	0	V_{PN}	0	0	$V_{PN}/3$
State 2	$-V_{PN}/2$	V_{PN}	V_{PN}	0	$V_{PN}/6$
State 3	0	0	V_{PN}	0	$V_{PN}/3$
State 4	$-V_{PN}/2$	0	V_{PN}	V_{PN}	$V_{PN}/6$
State 5	0	0	0	V_{PN}	$V_{PN}/3$
State 6	$-V_{PN}/2$	V_{PN}	0	V_{PN}	$V_{PN}/6$
State 7* ($V_2 \rightarrow V_7$)	$-V_{PN}/2$	$5V_{PN}/6$	$5V_{PN}/6$	$5V_{PN}/6$	$V_{PN}/3$
State 7* ($V_6 \rightarrow V_7$)	$-V_{PN}/2$	$5V_{PN}/6$	$5V_{PN}/6$	$5V_{PN}/6$	$V_{PN}/3$
State 7* ($V_4 \rightarrow V_7$)	$-V_{PN}/2$	$2V_{PN}/3$	$2V_{PN}/3$	$2V_{PN}/3$	$V_{PN}/6$

2.3. Proposed Logic-Function-Based PWM Generation

To ensure accurate control of the semiconductor switches in the SCB^{2}TSI structure for generating the CMV values calculated in Table 2, a modulation strategy combining the space vector approach with the proposed logic functions is presented in Fig. 6. Unlike the conventional SVPWM method implemented on the α – β plane, as illustrated in Fig. 7 a, which utilizes both zero vectors V_0 (000) and V_7 (111), the proposed modulation strategy for the SCB^{2}TSI configuration employs only a single zero vector V_7 (111) throughout the entire modulation cycle. When the reference vector $\overrightarrow{V_{ref}}$ lies in sector I, it is synthesized from two adjacent active vectors $\overrightarrow{V_1}$, $\overrightarrow{V_2}$ and one zero vector $\overrightarrow{V_7}$. The control signals *ma*, *mb* and *mc*, after being compared with a 10 kHz carrier wave and combined with the logic functions given in Table 3, correspond to the switching states of the SCB^{2}TSI is semiconductor switches, as depicted in Fig. 7 b. This approach reduces the switching frequency of certain semiconductor devices, thereby lowering switching losses and improving the overall efficiency of the system.

Table 3. Logic functions for the gate signals of the SCB^{2}TSI

$S_1 = (D_1 + D_2 + D_3)S_7$	$S_6 = \bar{S}_5$
$S_2 = \bar{D}_1\bar{D}_2\bar{D}_3$	$S_7 = \bar{S}_8$
$S_3 = (\bar{D}_1\bar{D}_2\bar{D}_3) + D_2$	$S_8 = D_1 + D_2 + D_3$
$S_4 = \bar{S}_3$	$S_A = (S_1 \oplus S_3 \oplus S_5)S_7$
$S_5 = (\bar{D}_1\bar{D}_2\bar{D}_3) + D_3$	$S_B = \overline{S_1 \oplus S_3 \oplus S_5} + S_8$

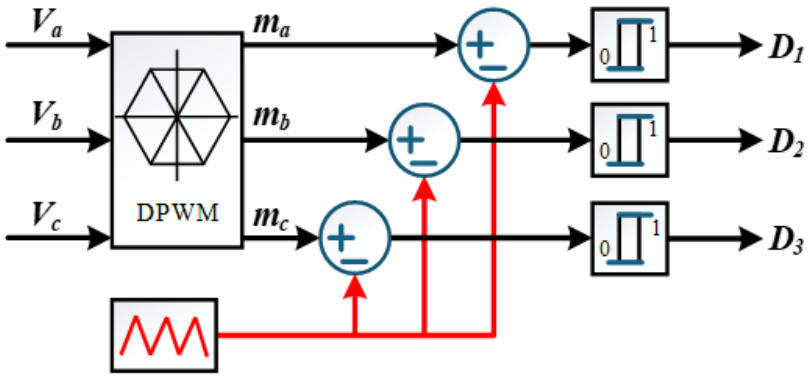


Fig. 6. Integral state feedback control system block diagram

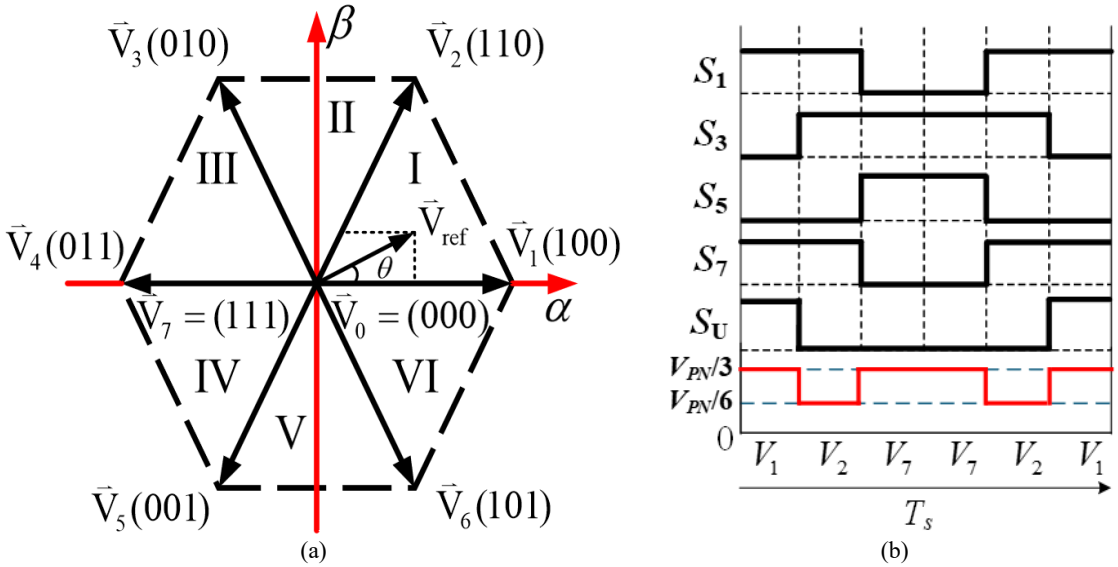


Fig. 7. Proposed strategy for the SCB²TSI: (a) Space vetor diagrams in the α - β plane, (b) modulation sequence for V_{ref} on sector 1 of the proposed scheme

3. Simulation Results

The configuration of the SCB²TSI combined with the logic-based space vector PWM strategy has been presented in the previous section. To evaluate the overall performance of this topology, a simulation model is developed in the PSIM environment. The simulation parameters listed in Table 4 are used to validate the proposed SCB²TSI. As shown in Fig. 8, the simulated waveforms include the input DC voltage, DC-link voltage, line-to-line voltage, and output current. Specifically, Fig. 8 a shows that the voltages across capacitors C_U and C_D are maintained at a balanced level of 110 V during operation. Consequently, the DC-link voltage of the proposed SCB²TSI structure reaches twice the input DC voltage of 220 V under the space vector PWM strategy, which employs a single zero vector V_7(111) combined with the logic function. In addition, Fig. 8 b indicates that the drain-source voltages of switches S_U and S_D are equal to the DC input voltage, while the voltages across diodes D_a and D_b exhibit symmetric amplitudes ($\pm V_{DC}$). This demonstrates that voltage balancing is effectively maintained and that the switched-capacitor stage operates correctly according to the intended design principle. The output waveforms of the SCB²TSI are shown in Fig. 8 c, with the corresponding fast fourier transform (FFT) analysis presented in Fig. 8 d. At a modulation index of Mi = 0.9, the line-to-line output voltage exhibits a unipolar waveform with a fundamental component amplitude of 198 V, while the phase-to-neutral voltage presents a staircase profile. The output line-to-line voltage has an RMS value of 140 V with a total harmonic distortion (THD) of about 0.28%, while the output current reaches 1.15 Arms with a THD of about 0.3%.

Table 4. Simulation parameter

Parameters	Values
Power rating	500 W
DC supply (V_{DC})	110 V
DC capacitance (C_U, C_D)	470 µF
Switching frequecy (f_{sw})	10 kHz
Filter inductance (L_f)	3 mH
Filter capacitance (C_f)	10 µF
Load (R)	75 Ω

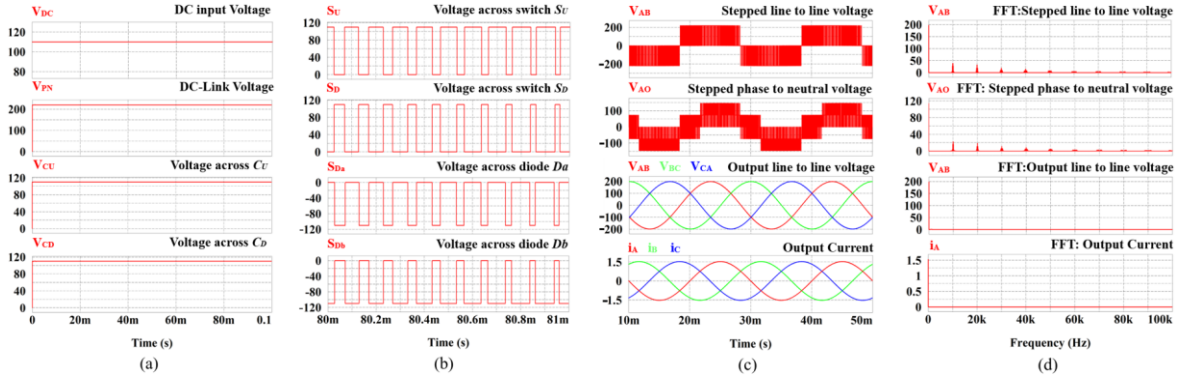


Fig. 8. Waveforms of the proposed topology. From top to bottom: (a) DC input voltage, DC-Link voltage, voltage across C_U and voltage across C_D, (b) Voltage across switch S_U, Voltage across switch S_D, Voltage across diode D_a and Voltage across diode D_b, (c) Stepped line-to-line voltage, stepped phase-to-neutral voltage, output line-to-line and output current, (d) FFT of stepped line-to-line voltage, FFT of stepped phase-to-neutral voltage, FFT of ouput line-to-line voltage and FFT of output current

Fig. 9 and Fig. 10 present the simulation results corresponding to modulation index Mi = 0.9 and Mi = 0.6. In Fig. 9 a and Fig. 10 a, the phase-to-ground voltages (V_{AM}, V_{BM}, V_{CM}) and the CMV are clearly illustrated. Fig. 9 b and Fig. 10 b show enlarged views of the corresponding V_{CMV} waveforms. It can be observed that the phase voltages exhibit a stepped waveform, varying from −100 V to 200 V. Meanwhile, the CMV during powering modes fluctuates between V_{PN}/6 and V_{PN}/3, and remains within the same range during freewheeling modes. These results confirm that the proposed SCB^{2}TSI maintains the CMV within a narrow fluctuation range of V_{PN}/6 to V_{PN}/3, regardless of variations in the modulation index from Mi = 0.6 to Mi = 0.9. Table 5 provides an overview of the common-mode voltage mitigation voltage mitigation capability of previously reported inverter topologies and

Table 5. Comparison between the proposed SCB^{2}TSI and other inverter topologies with the same DC-link voltage (V_{PN})

Topology	Switches + Diodes* + Capacitor*	DC voltage supply	Boost Capability	Overall variation in CMV	*Mi* Range
Conventonal Three phase inveter with SVPWM	6 + 0 + 0	$2V_{DC}$	No	0 to V_{PN}	0 to 1
Conventonal Three phase inveter with NSPWM [46]	6 + 0 + 0	$2V_{DC}$	No	V_{PN}/3 to 2V_{PN}/3	0.6 to 1
Conventonal Three phase inveter with HSVPWMS [48]	6 + 0 + 0	$2V_{DC}$	No	-V_{PN}/3 to V_{PN}/3	0 to 1
H7 topology [52]	7 + 0 + 1	$2V_{DC}$	No	V_{PN}/3 to V_{PN}	0 to 1
H7 topology [53]	7 + 6 + 1	$2V_{DC}$	No	V_{PN}/3 to 2V_{PN}/3	0 to 1
H8 topology [54]	8 + 0 + 1	$2V_{DC}$	No	V_{PN}/3 to 2V_{PN}/3	0 to 1
H8 topology [56]	8 + 0 + 0	$2V_{DC}$	No	V_{PN}/3 to 2V_{PN}/3	0 to 1
H10 topology [55]	10 + 0 + 1	$2V_{DC}$	No	V_{PN}/3 to 2V_{PN}/3	0 to 1
H10 topology [57]	10 + 0 + 1	$2V_{DC}$	No	V_{PN}/3 to 2V_{PN}/3	0 to 1
Proposed SCB^{2}TSI topology	10 + 2 + 2	V_{DC}	Yes	V_{PN}/6 to V_{PN}/3	0 to 1

*The intrinsic body diodes and junction capacitances are excluded from the component count

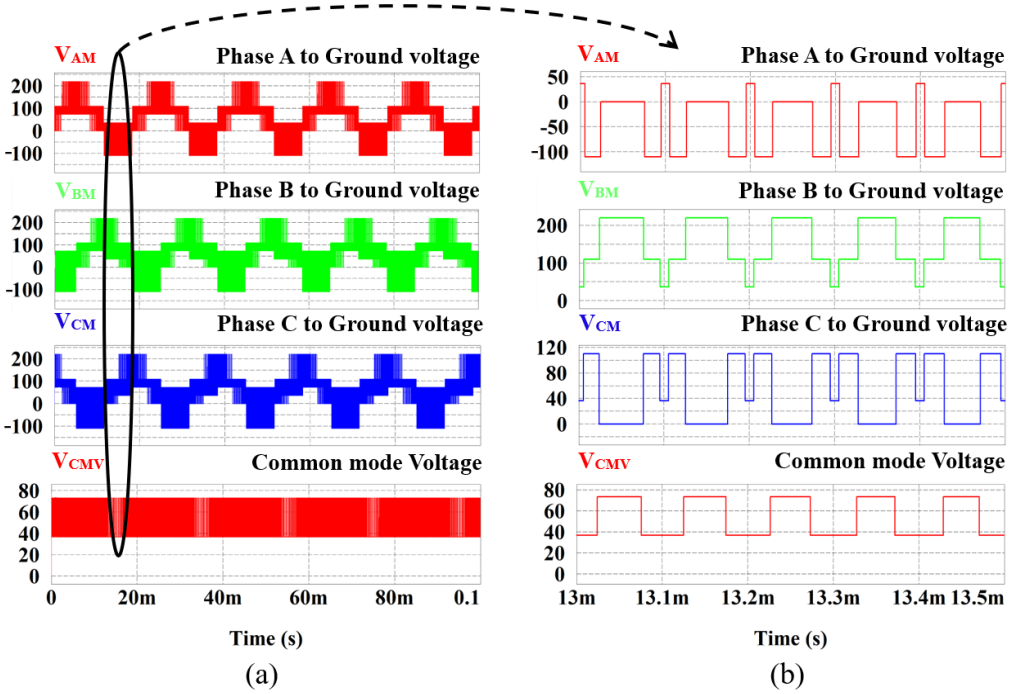


Fig. 9. Phase-to-ground voltage and CMV of proposed inverter at modulation index Mi = 0.9. From top to bottom: (a) Phase A to ground voltage, Phase B to ground voltage, Phase C to ground voltage and common mode voltage, (b) Zoomed view of common-mode voltage waveform

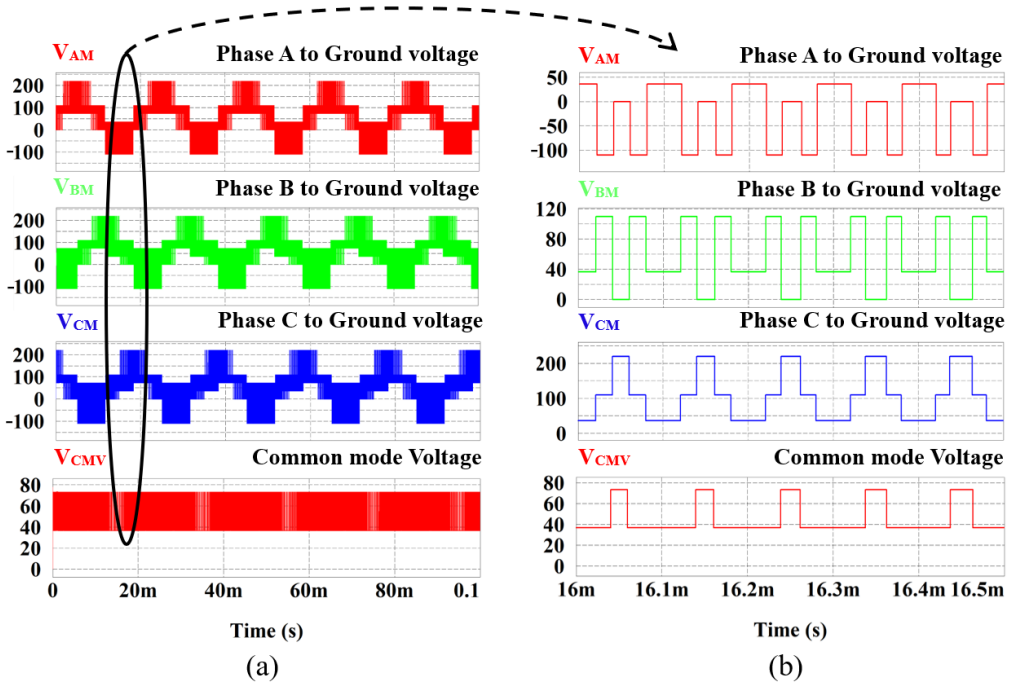


Fig. 10. Phase-to-ground voltage and CMV of proposed inverter at modulation index Mi = 0.6. From top to bottom: (a) Phase A to ground voltage, Phase B to ground voltage, Phase C to ground voltage and common mode voltage, (b) Zoomed view of common mode voltage waveform

Compares them with the proposed SCB^{2}TSI configuration. The evaluation criteria include the number of power switches, diodes, and capacitors employed in each topology, with particular emphasis on the CMV fluctuation range relative to the DC-link voltage. This comparison highlights the effectiveness of the proposed SCB^{2}TSI in maintaining CMV within a narrow range from $V_{PN}/6$ to $V_{PN}/3$, while simultaneously achieving a voltage-doubling feature of the DC-link compared with other

inveter topologies. Therefore, the proposed topology demonstrates high potential for practical applications in modern power conversion and motor drive systems.

4. Experimental Results

To validate the CMV reduction capability and effectiveness of the proposed SCB^{2}TSI topology, an experimental prototype was developed. A current-limiting resistor is employed at the DC input to mitigate inrush current during start-up, while the gate driver circuit based on the HCPL-316J provides desaturation detection and short-circuit protection for the power devices. The experimental parameters are kept identical to those used in the simulation.

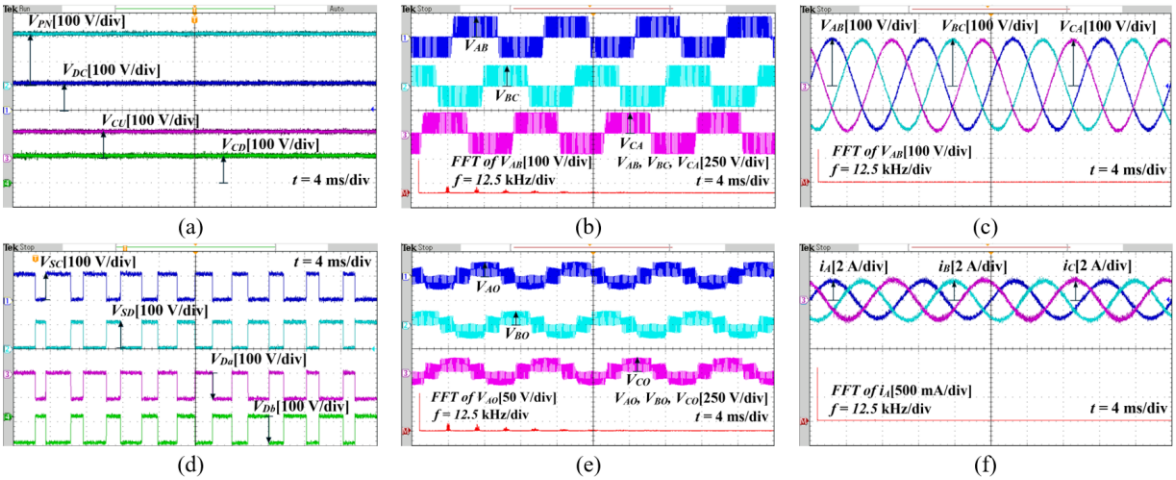
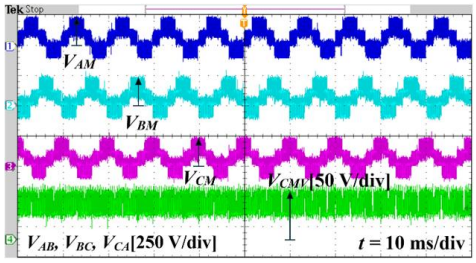


Fig. 11. Experimental results of the proposed SCB^{2}TSI topology. From top to bottom: (a) DC-link voltage, Input DC voltage, Voltages across capacitors C_U and C_D, (b) Line-to-line voltage V_{AB}, V_{BC}, V_{CA} and their FFT analyis, (c) Output line-to-line voltage V_{AB}, V_{BC}, V_{CA} and their FFT analyis, (d) Voltages across switch S_U and S_D, voltages across diode D_a and D_b, (e) Phase-to-neutral voltage V_{AO}, V_{BO}, V_{CO} and their FFT analyis, and (f) Output currents and FFT of output current

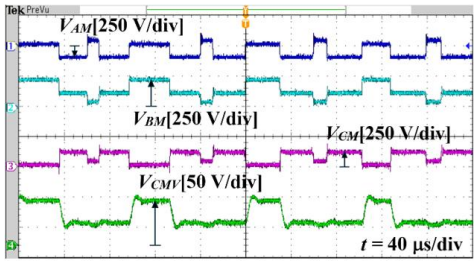
Fig. 11 presents the experimental results of the proposed SCB^{2}TSI configuration, including the input DC voltage, DC-link voltage, voltage across diodes D_a and D_b, drain-source voltages of switches S_C and S_D, as well as the line-to-line voltage and output current waveforms with FFT analysis. As highlighted in Fig. 11 a, when the DC input voltage is set to 110 V, the DC-link voltage is boosted to 220 V, which is fully consistent with the simulation result and theoretical analysis. Fig. 11 d illustrates the drain–source voltages of switches S_C and S_D, with amplitudes approximately equal to the DC supply voltage of 110 V, highlighting their role in controlling the charging and discharging processes of the two switched-capacitor cells. The corresponding voltage waveforms across diodes D_a and D_b confirm that current conduction occurs during the intended operating intervals, ensuring proper current paths in each switching state. The complementary operation of switches S_C and S_D enables alternating energy transfer between the input source and the capacitor cells, thereby preventing voltage drift and maintaining balanced capacitor voltages. These experimental observations indicate that the voltage stress across the power semiconductor devices remains within safe operating limits and that the system operates reliably and robustly under practical experimental conditions. Compared with the simulation results in Fig. 8 c, Fig. 11 b shows that the line-to-line voltages V_{AB}, V_{BC}, V_{CA} exhibit stepped varying from −198 V to 198. As observed in Fig. 11 e, the phase-to-neutral voltages exhibit a distinct staircase waveform, where the fundamental component is 79 Vrms. Finally, Fig. 11 e illustrates the post-LC-filter results, showing that the line-to-line voltages V_{AB}, V_{BC}, V_{CA} achieve 140 Vrms with a total harmonic distortion of approximately 0.3%, while the output current reaches 1.1 Arms with a THD of about 0.32%.

Fig. 12 and Fig. 13 present the experimental results of the phase-to-ground voltages V_{AM}, V_{BM}, V_{CM} and the CMV of the proposed SCB^{2}TSI topology. Specifically, in Fig. 12 a with a modulation

index of Mi = 0.9, the phase-to-ground and CMV waveforms are recorded, while the magnified view in Fig. 12 b shows that the CMV oscillates within the range of $V_{PN}/6$ to $V_{PN}/3$. Similarly, at Mi = 0.6, the experimental results shown in Fig. 13 a and Fig. 13 b confirm that the CMV remains in the same range of $V_{PN}/6$ to $V_{PN}/3$. These results are consistent with the simulation, confirming that the SCB^{2}TSI topology maintains stable CMV characteristics even when the modulation index varies from 0.6 to 0.9. Compared with conventional H8-based inverters and H10-based inverters reported in [52]-[57], the proposed SCB^{2}TSI topology avoids the need for an additional front-end DC–DC boost stage, thereby reducing overall power loss and improving system-level efficiency. Moreover, the inherent capacitor self-balancing and constrained CMV operation contribute to stable experimental waveforms and reliable operation.

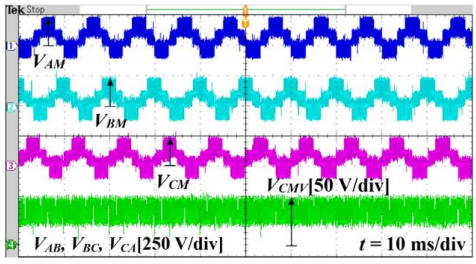


(a)

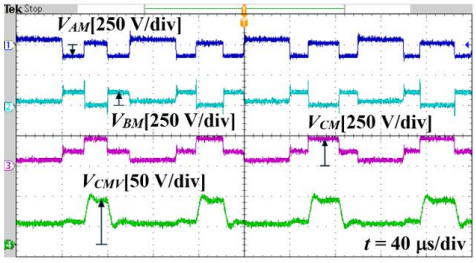


(b)

Fig. 12. Experimental results of the proposed SCB^{2}TSI topology at modulation index Mi = 0.9. From top to bottom: (a) Phase-to-ground voltage V_{AM}, V_{BM}, V_{CM} and common mode voltage, (b) Zoomed view of phase-to-ground voltage and common mode voltage waveform



(a)



(b)

Fig. 13. Experimental results of the proposed SCB^{2}TSI topology at modulation index Mi = 0.6. From top to bottom: (a) Phase-to-ground voltage V_{AM}, V_{BM}, V_{CM} and common mode voltage, (b) Zoomed view of phase-to-ground voltage and common mode voltage waveform

5. Conclusion

This paper presents the analysis, simulation, and experimental validation of the proposed SCB^{2}TSI topology, which is developed from the ten-switch configuration integrated with a switched-capacitor boost network. In the proposed structure, the alternate charging and discharging processes of capacitors C_U and C_D enables the DC-link voltage supplied to the inverter stage to be doubled with respect to the input DC voltage. However, this voltage-boosting mechanism introduces a design trade-off in terms of increased component count, higher circuit complexity, and the need for careful capacitor sizing to ensure reliable operation. Moreover, the common-mode voltage amplitude is constrained to V_{PN}/6 and V_{PN}/3 levels by employing a pulsewidth modulation strategy combined with the corresponding logic controller. The results indicate that the CMV amplitude is limited to only 16.66% of the DC-link voltage. This approach not only achieves a significant reduction in CMV, thereby enhancing operational safety in transformerless photovoltaic systems, but also demonstrates strong suitability for industrial electric drive applications, where reduced leakage current contributes to extended motor lifetime and lower maintenance costs. Future work will focus on extending the proposed topology to higher power ratings, as well as further optimizing switching losses and capacitor parameter selection to improve overall system performance.

Author Contribution: All authors contributed equally to the main contributor to this paper. All authors read and approved the final paper.

Funding: This research received no external funding.

Conflicts of Interest: The authors declare no conflict of interest.

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